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SIDE-LOBE CANCELLER
IF RECEIVER DESIGN

FINAL DESIGN REPORT

April 1993 V1.2 John Curnow

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April 1993 V1.2

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1.0 INTRODUCTION

This is the final design report for the Side-Lobe Canceller (SLC) 60 MHz IF receiver system. It presents the detailed designs and calculations for each section of the IF receiver.

The RF, or front end, portion of the SLC receiver resides on a large horizontal plate in the front end equipment rack. Figure One is a block diagram of the Experimental Array Radar System (EARS), including the SLC receiver. This system configuration is temporary and will be changed with the integration of the new data acquisition system and system controller. In Figure One the Slow Speed Sample and Hold and SSTP are used to acquire the I and Q data from the SLC receiver. The new data acquisition system will be used in the near future to digitize the offset video outputs of the SLC receiver.

Figure Two is a block diagram of a single channel of the complete SLC system. The IF receiver boards mix the IF mixer signal and a 60 megahertz reference signal from the Exciter to produce the in phase (I) and quadrature (Q) baseband signals. The I and Q signals from the quadrature detector section pass through low pass filters and amplifiers. The filters eliminate harmonics and noise, to improve the signal-to-noise ratio. The output amplifiers provide additional signal level and current to drive 50 ohm coaxial lines. The eight I and eight Q signals go to the data acquisition system. The IF receiver boards also provide 60 MHz IF outputs for future digitization and offset video outputs.

1.1 SLC RF Receiver Description

Figure Three is a block diagram of the front end of the SLC receiver. The SLC array is composed of eight Narda Model 640 standard gain horns mounted horizontally, using horizontal polarization. The horns are mounted as close as the mechanical tolerances permit. Each horn feeds a low noise amplifier (LNA) through a waveguide to SMA transition. The output of each LNA goes into one input port of a beam forming network (BFN) through a phase shifter. The BFN is an optional device in the SLC system. It integrates the eight inputs into the eight outputs. Each output yields a different azimuth direction for the receiver.

The low noise amplifiers are mounted on the antenna bracket, directly behind each horn. They are model AMF-2S-085100-20 by Miteq Inc. The two most important specifications are the gain and the noise figure. The minimum gain over the 8.5 GHz to 10.0 GHz range is 19.6 decibels. The maximum noise figure over this frequency range is 1.8 decibels, although it is typically less than 1.4 dB. The one decibel compression point is +10 dBm.

Small phase imbalances will exist between the front end channels due to component tolerances and the coaxial cables. To

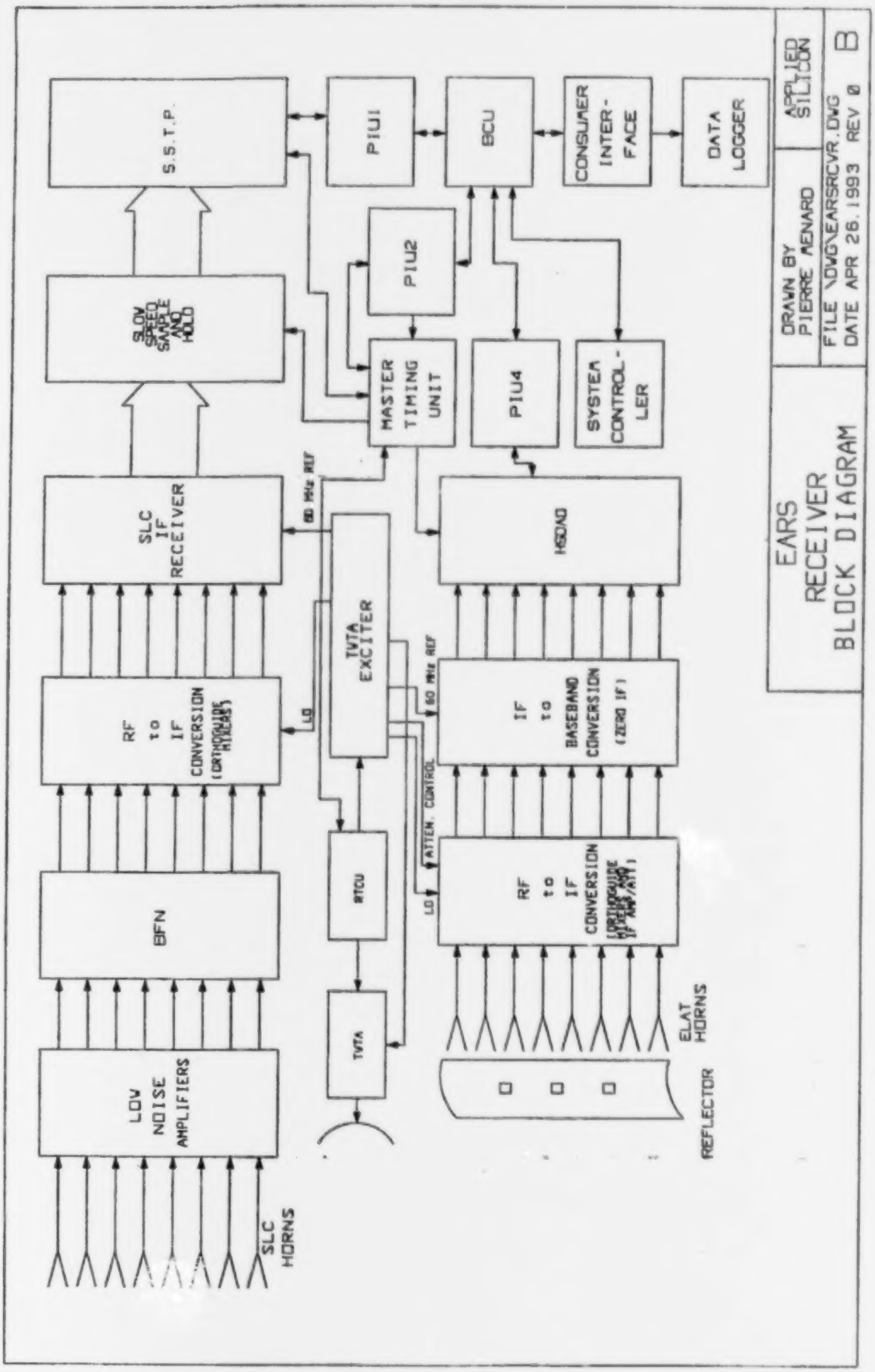

SLC HORNS
LOW NOISE AMPLIFIERS
BFN
RF to IF CONVERSION (ORTHOGUIDE MIXERS)
SLC IF RECEIVER
SLOW SPEED SAMPLE AND HOLD
S.S.T.P.
PIU1
BCU
CONSUMER INTER-FACE
DATA LOGGER
PIU2
MASTER TIMING UNIT
PIU4
SYSTEM CONTROL-LER
60 MHz REF
LO
TWTA EXCITER
RTCU
TWTA
HSDAD
IF to BASEBAND CONVERSION (ZERO IF)
60 MHz REF
ATTEN. CONTROL
LO
RF to IF CONVERSION (ORTHOGUIDE MIXERS AND IF AMP/ATT)
ELAT HORNS
REFLECTOR
EARS RECEIVER BLOCK DIAGRAM
DRAWN BY PIERRE MENARD
FILE \DWG\EARSRCVR.DWG
DATE APR 26,1993 REV 0
APPLIED SILICON
B

Figure 1

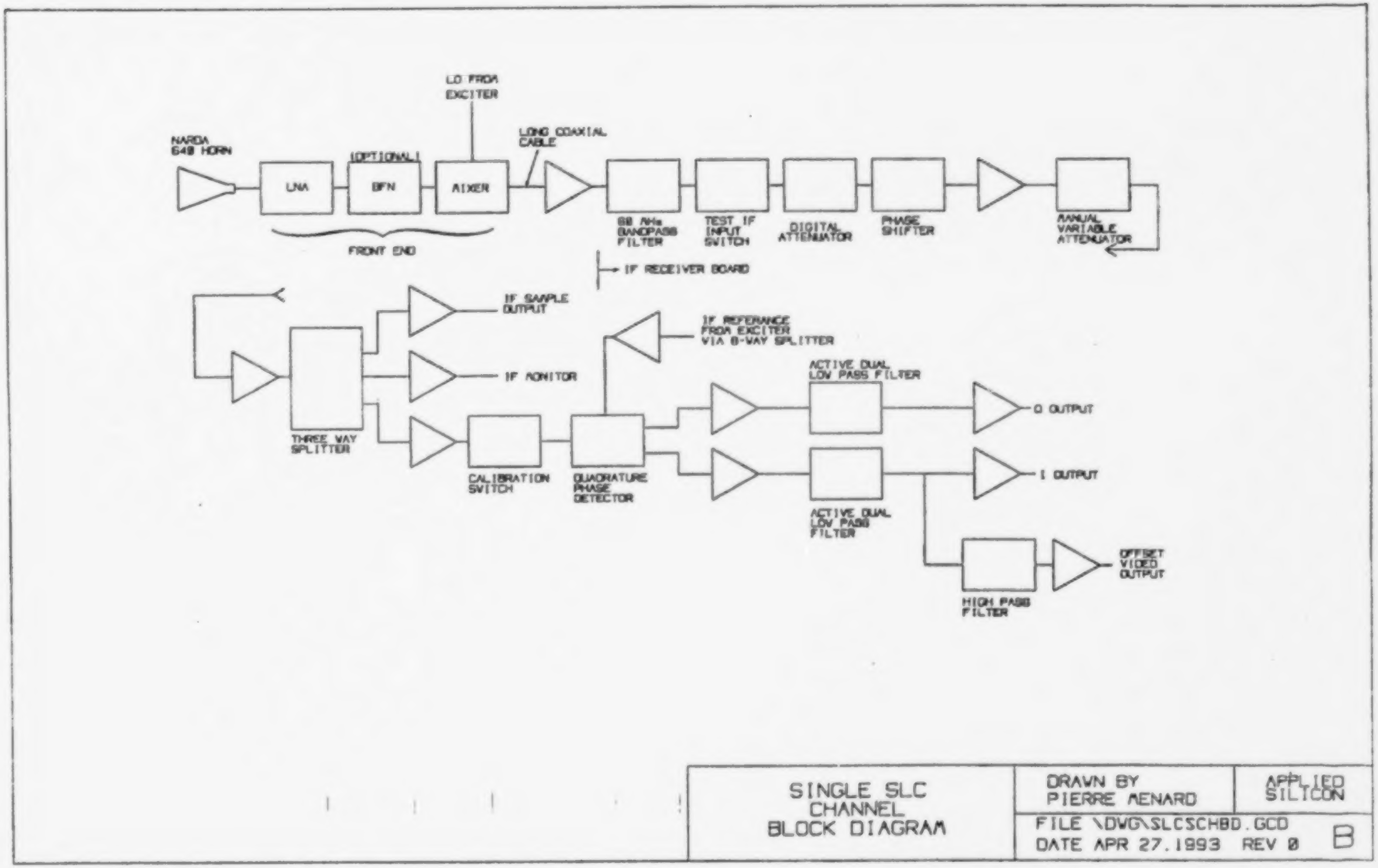

LO FROM EXCITER
NARDA 640 HORN
(OPTIONAL)
LNA
BFN
MIXER
FRONT END
LONG COAXIAL CABLE
60 MHz BANDPASS FILTER
TEST IF INPUT SWITCH
DIGITAL ATTENUATOR
PHASE SHIFTER
MANUAL VARIABLE ATTENUATOR
IF RECEIVER BOARD
IF SAMPLE OUTPUT
IF MONITOR
THREE WAY SPLITTER
CALIBRATION SWITCH
QUADRATURE PHASE DETECTOR
IF REFERANCE FROM EXCITER VIA 8-WAY SPLITTER
ACTIVE DUAL LOW PASS FILTER
ACTIVE DUAL LOW PASS FILTER
Q OUTPUT
I OUTPUT
HIGH PASS FILTER
OFFSET VIDEO OUTPUT
SINGLE SLC CHANNEL BLOCK DIAGRAM
DRAWN BY PIERRE MENARD
APPLIED SILTCON
FILE \DWG\SLCSCHBD.GCD
DATE APR 27.1993 REV 0
B

FIGURE 2

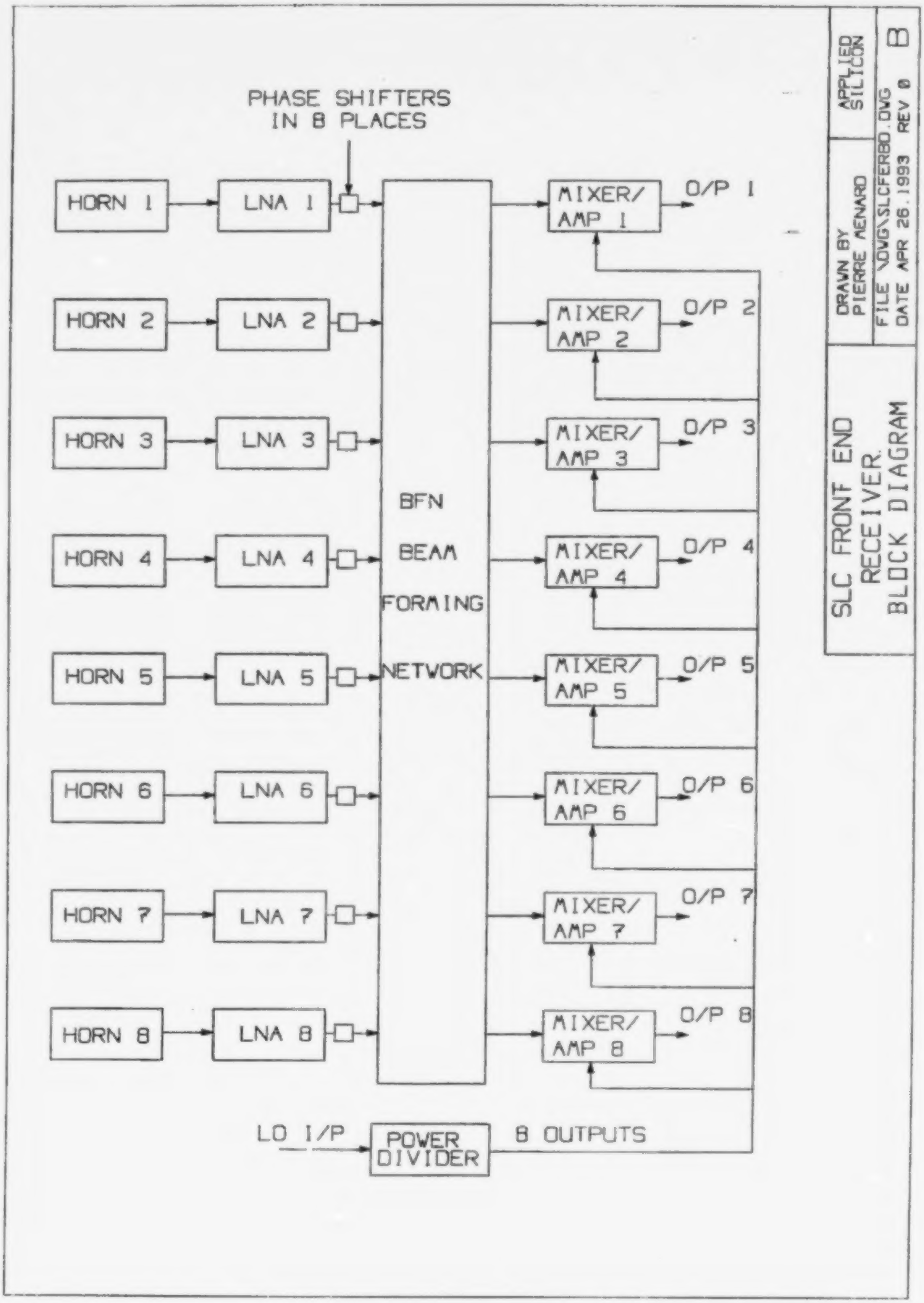

PHASE SHIFTERS
IN 8 PLACES
HORN 1
HORN 2
HORN 3
HORN 4
HORN 5
HORN 6
HORN 7
HORN 8
LNA 1
LNA 2
LNA 3
LNA 4
LNA 5
LNA 6
LNA 7
LNA 8
BFN
BEAM
FORMING
NETWORK
MIXER/ AMP 1
MIXER/ AMP 2
MIXER/ AMP 3
MIXER/ AMP 4
MIXER/ AMP 5
MIXER/ AMP 6
MIXER/ AMP 7
MIXER/ AMP 8
O/P 1
O/P 2
O/P 3
O/P 4
O/P 5
O/P 6
O/P 7
O/P 8
LO I/P
POWER DIVIDER
8 OUTPUTS
APPLIED SILICON
B
DRAWN BY PIERRE MENARD
FILE \DWG\SLCFERBD.DWG
DATE APR 26.1993 REV 0
SLC FRONT END RECEIVER BLOCK DIAGRAM

Figure 3

reduce the phase differences small manual control phase shifters are used in the lines between the LNAs and the BFN. The phase shifters are CDI model 5999-1 phase adjustable SMA connectors. At a frequency of ten gigahertz the adjustment range is 49 degrees.

The BFN is a Rotman Lens. There are 24 input ports and 15 output ports. In the SLC system every third input connector and every second output are used. The scan sector is covered by eight beam positions that are equally spaced in sine theta space. The insertion loss is tested at 17 dB to 20 dB from any single input to any output. The insertion loss of the eight summed inputs to any output is about ten decibels.

The mixers are made by RHG and are model WM8-12/15. They are of the orthoguide type, with the RF input in a WR90 waveguide and the IF output in an SMA connector. The LO also uses an SMA connector. An SMA to waveguide transition is used on the RF input. The mixers have a maximum IF output of 0 dBm at the one decibel compression point and a maximum specified noise figure of 7.7 dB. Their minimum tested RF to IF gain is 21 dB.

2.0 SLC IF RECEIVER SPECIFICATIONS

The design requirements called for the SLC receiver to match or better the Zero IF (ZIF) specifications. The SLC receiver actually combines the functionality of the ZIF and the IF Amplifier/Attenuator (IF A/A). The IF A/A has sections for digital control of attenuation and IF amplification. It was not possible to meet all of the specifications for the ZIF or IF A/A. The requirements of the SLC array are different from the main UAE200 array, so it is not applicable to match all the specifications for the two systems. The main design specifications for the SLC receiver are;

Signal Frequency	60 MHz +/-5 MHz
IF Gain	62 dB +/-1 dB maximum
Gain Control Range	62 dB
IF Gain Tracking	+/-2.0 dB @ 60 MHz, 0 to 62 dB atten.
IF Gain Matching	+/-0.5 dB @ 60 MHz
IF Phase Tracking	+/-5 degrees @ 60 MHz, 0 to 62 dB atten.
IF Phase Matching	+/-2 degrees @ 60 MHz
Video Bandwidths	1.4 MHz, 6.0 MHz, switch selected
I and Q Output Level	10 volts peak to peak, 50 Ω
Offset Video Output Level	5 volts peak to peak, 50 Ω
Video I/Q Level Balance	< 0.5 dB
Video I/Q Phase Balance	90 degrees +/-2 degrees @ 1 MHz
DC Offset, no signal	< 5 mV @ 20 degrees Celsius
Video Noise	< 200 μV RMS

3.0 GENERAL DESCRIPTION

The Side-Lobe Canceller IF receiver consists of a series of eight identical boards, one for each channel of the SLC array. Each board is capable of producing one I and one Q output at a level that is suitable for digitizing by a data acquisition system. In addition, the boards provide monitor points and a high level 60 megahertz output, suitable for future digital sampling. Each board also has an offset video output, with a bandwidth of one to six megahertz. The multiple outputs increase the complexity of the receiver boards but also make them more versatile by allowing three methods of producing the information.

The receiver enclosure is mounted in a rack in the portable laboratory, close to the data acquisition systems. The eight channel receiver boards are mounted in a double height eurocard rack, with a ninth board for the computer interface, reference amplifier and splitter. Adequate shielding is provided to prevent cross talk and coupling. The high level reference signal in particular is well shielded to prevent it from interfering with the lower level IF and video signals. All IF and video connections are made at the rear of the enclosure, with a backplane assembly for power and control signals.

All of the IF components on the receiver channel board have a nominal 50 ohm input and output impedance. All of the active devices in the IF chain are AC coupled using 1 nF capacitors. In a fifty ohm system this gives a high pass corner frequency of about 3.2 MHz. The channel can be divided into about fourteen sub-sections to simplify the design and description. Section four of this report contains a design description of each sub-section.

4.0 CIRCUIT DESIGN DESCRIPTIONS

This section describes each sub-section of the receiver design in detail. It presents the design rationale and calculations for each device or part in the receiver. The reader should refer to the main circuit schematics contained in Appendix B while reading. The components are presented in order from the 60 MHz inputs through to the various outputs.

4.1 Input Amplifier and Bandpass Filter

The low level 60 MHz IF signal from the orthoguide mixers can be attenuated by a three decibel resistor T-pad. This provides a 50 ohm impedance and reduces the level by three decibels to reduce reflections caused by mismatches through the cables and connectors. It also increases the noise figure and so is provided as an option, to be used only if necessary. The first gain stage is a MAN-1HLN amplifier by Mini-Circuits (MCL). It is a fixed gain block with a gain of about 12 decibels at 60 megahertz. The manufacturer's specifications are in Appendix A. It has a noise figure of only

3.9 dB and a one decibel compression point of +17.4 dB at 60 megahertz. In this application, the one decibel compression point of the mixer will be reached before the first gain stage begins to compress. The noise generated by the first gain stage should be less than the noise output of the front end mixer.

To calculate the output noise of an active RF device, the following formula is used;

$$\text{Noise Out} = N_o = F\ k\ T_o\ B_n\ G$$

where F = linear noise figure
k = Boltzman's Constant = 1.38×10^{-23}
T_o = temperature in Kelvin = 273 K + 20°C = 293 K
B_n = bandwidth in hertz
G = linear gain

For the MAN-1HLN, the linear gain is 15.85 and the linear noise figure is 2.455. Inserting the numbers into the above equation gives an output noise of 7.87×10^{-11} watts.

Since 0 dBm = 1×10^{-3} watts, 7.87×10^{-11} watts = -71.0 dBm. This translates to an equivalent input noise of -83 dBm.

The tested parameters for the WM8-12/15 mixer/preamp are;

noise figure = 7.5 dB maximum (5.62 linear)
minimum gain = 21 dB (125.9 linear)
bandwidth = 10 megahertz

Inserting the WM8-12/15 parameters into the above noise equation yields an output noise of -75.4 dBm. This translates to an equivalent input noise of -75.4-21 dB gain = -96.4 dBm. The output noise of the mixer/preamp will be attenuated over the long coaxial run from the front end by about -2.5 dB. Therefore, at the MAN-1HLN IF input the noise contribution from the WM8-12/15 mixer/preamp is -75.4-2.5 = -77.9 dBm. This is well above the equivalent input noise level of -83 dBm from the MAN-1HLN.

A 60 MHz bandpass filter follows the first gain stage. The filter reduces harmonics or spurious signals which may exist outside the IF band of interest. These unwanted signals can interfere with the 60 MHz IF signal and increase the noise level. A passive LC filter design was chosen. The design is a standard bandpass filter using full-section pi networks. It uses only three inductors and three capacitors. This configuration is not as complex as the bandpass filter used in the ELAT IF Amplifier/Attenuator. It requires only two variable elements for proper tuning. It does not have the same delay or tight group delay specifications, although it is close. The design and formulas can be found in the book, "Simplified Practical Filter Design" by Irving M Gottlieb.

Figure Four shows the configuration of the 60 MHz bandpass filter. The critical components are L1 and C1 and these should be variable to tune the center of the filter to 60 MHz. The formulas to calculate the individual values are shown following Figure Four.

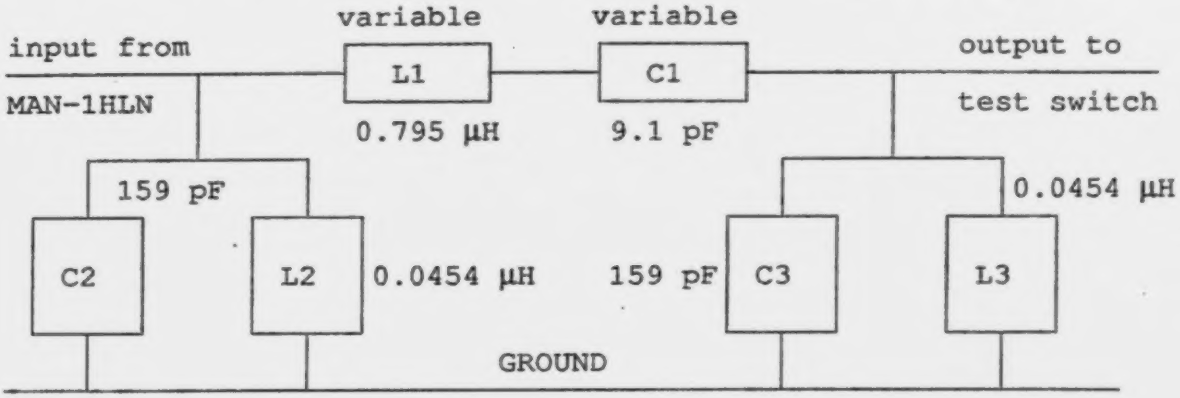


Figure Four

60 MHz Bandpass Filter

$$L1=\frac{R}{\pi(f_2-f_1)} \qquad L2=L3=\frac{R(f_2-f_1)}{2\pi(f_2\times f_1)}$$

$$C1=\frac{f_2-f_1}{4\pi(f_2\times f_1)R} \qquad C2=C3=\frac{1}{2\pi(f_2-f_1)R}$$

With a three decibel bandwidth of 20 MHz and a centre frequency of 60 MHz, f_1=50 MHz and f_2=70 MHz. R is the input and output impedance which is 50 ohms. Putting these numbers into the equations yields the values shown in the filter diagram. An AC analysis of this filter was run on ACNAP, an analysis program from BV Engineering. The exact calculated values were used and the result was as expected. The nearest standard values for C2, C3, L2 and L3 were analyzed also. These were C2=C3=160 pF and L2=L3=0.047µH. The results were good when L1 and C1 were tuned to the proper values. A prototype filter was built up, using wide tolerance components. The tested delay at 60 MHz was 31.8 nS, with a group delay variation from 31.8 nS at 55 MHz to 37.9 nS at 65 MHz. The 3 dB bandwidth was 20 MHz and the 20 dB bandwidth was 42.5 MHz. The insertion loss was almost 3 decibels. These results are close to the IF Amplifier/Attenuator filter specifications.

4.2 IF Test Switch

A PSW-1211 switch by Mini-Circuits is used after the 60 MHz bandpass filter. This is to allow the introduction of a 60 MHz IF test signal into the circuit. It is an SPDT configuration wide band pin diode switch with a minimum in-out isolation of 40 decibels. It does not have internal TTL drivers. It is controlled by a front panel toggle switch, located on the control board. The toggle switch controls all eight test switches in parallel. The IF test input is AC coupled and can have an amplitude of up to +10 dBm without saturating the receiver.

4.3 Digital Attenuator

The digital attenuator section is used to compensate for the varying input signal level and extend the dynamic range of the receiver. It was judged that a minimum step size of one decibel is not necessary. Trial experience with the ELAT system using the SPAR IF Amplifier/Attenuator has shown that a minimum step size of two or three decibels is adequate. Using a step size of two decibels will allow the use of a single attenuator package and still permit a wide enough attenuation range. Using a single attenuator package keeps the cost in line and increases the attenuation accuracy.

The attenuator chosen is built by Daico Industries, model DA0857. It has five sections, a resolution of 2 decibels, a range of 62 dB and an absolute maximum error of 1.49 dB. It does not require a separate logical interface since the step sizes are 2,4,8,16 and 32 decibels, with a TTL interface. Buffer drivers are required between the control computer and the attenuators.

4.4 Phase Adjustment

Each receiver channel will cause a different phase shift of the 60 MHz IF signal. This is mainly due to variable line lengths and individual component tolerances. In order to reduce the phase differences to the specified level, some type of phase shifter must be used. Previous receivers used external manually variable phase shifters. This requires a particular test setup to adjust the phase shifters and takes at least half a day to do the adjustment. The phase differences will change over time due to temperature effects and aging of components, so frequent phase calibrations are necessary to keep the channel-to-channel phase differences less than two degrees.

To increase the phase adjust accuracy a design using a voltage variable phase shifter (VVPS) was carried out. Several models of VVPS devices were investigated. Most were rather expensive, although a relatively inexpensive model was found by Synergy Microwave Corporation. It is the model PP-902 VVPS in the plug-in package. The phase versus control voltage curve is in included in

Appendix A. Although up to 30 volts can be applied as the control voltage, the useful range is from 0 to 10 volts.

There are two ways to introduce the control voltage to the VVPS, either by computer control or by manual control. A small DIP package relay is used to switch between the two control voltages. The relay is controlled by a toggle switch, mounted on the front panel of the control board. Under manual control a potentiometer is used to vary the voltage tap from a precision reference. The reference contains a precision zener diode and a heater. Manual control will be used until the complete hardware and software system is in place to enable automated computer control. The manual control procedure will be similar to that used with past receiver systems.

Automated computer control will be implemented using a new data acquisition system. The control board has two DIP packages, each with four twelve bit digital to analogue converters (DAC). Each DAC controls one of the VVPSs. The connection between each DAC and VVPS is via coaxial cables to reduce noise pickup. Under computer control, using special software, each channel can be IF phase equalized quickly before a trial data collection. The description of the DAC's and computer interface is in section five.

After the phase shifter a second IF gain stage is used. It is a Signetics NE5204 fixed nominal 19 decibel gain IF amplifier. This amplifier is inexpensive but has good specifications, with a noise figure of 6.25 dB, a one decibel compression point of +8.5 dBm and a typical bandwidth of 550 MHz. Its maximum recommended supply voltage is +8 VDC. Rather than use a separate eight volt regulator, the +12 VDC supply is used with a dropping resistor. This sets the voltage at the supply pin to a nominal eight volts and isolates the supply from the amplifier, permitting better supply filtering. Although the dropping resistor wastes some power, it does eliminate a separate supply voltage along with its board tracks and regulator.

A noise calculation can be made for the NE5204 using the equation presented in section 4.1. The linear noise figure is 4.217 and the linear gain is 79.4. Using a bandwidth of 550 MHz, the noise generated by the NE5204 is -61.3 dBm at the output. This translates to an equivalent input noise of -80.3 dBm.

4.5 Manual Variable Attenuator

Each IF channel will have a different overall gain due to component tolerances and resistances in the cables and tracks. These imbalances must be removed to equalize the gains. The method to do this is to use external manually variable attenuators. A test IF signal is introduced to each channel at the output of the front end mixers. A similar procedure can be followed to adjust the SLC IF receiver. The attenuators are all adjusted to a near minimum value. The channel with the least gain is identified. The other seven channels are then attenuated to equal the least gain channel. This procedure takes about half a day and is usually done just before a series of trials.

It was decided to use the manual attenuator method to control the channel-to-channel gain imbalances. The alternative was to have an automated computer controlled adjustment, similar to the phase shift adjustments. The gain balances are not as critical as the phase balances and are not as sensitive to changes over time, so a complex computer controlled gain adjustment is not necessary. Rather than external variable attenuators, it is better to incorporate the attenuators directly onto the receiver board, at an appropriate point in the IF chain. The attenuators are accessible from the rear of each receiver board. They are adjusted with a screw thread and have a locking nut.

Immediately following the manual attenuator is another NE5204 amplifier. This provides a third gain block of 19 decibels. It is the same configuration as the first NE5204 after the phase shifter.

4.6 Three Way Splitter and IF Monitor

A DCP-2B2 three way zero degree splitter by Synergy Microwave follows the third gain block. It divides the IF signal into three equal signals, each at 5.3 decibels below the input. One of the output paths is used for an IF monitor. A MAN-1HLN amplifies the monitor output to a high level, equal to the IF sample output level. The monitor output will typically be around +10 dBm. The MAN-1HLN can drive up to +17.4 dBm into 50 ohms. It is AC coupled on the input and output.

An amplifier is used for the IF monitor point in order to produce a strong high level signal into 50 ohms. It isolates the IF monitor output from the other signal paths, to eliminate interference. If the monitor point is not connected, or improperly connected it should not cause problems for the other two signal paths out of the three way splitter. The monitor is brought out to the front panel of each receiver board on a BNC connector.

4.7 IF Sample Output

One of the outputs of the three way zero degree splitter is for a 60 MHz IF sample output. A MAN-1HLN 12 dB gain amplifier increases the signal to a level suitable for digital sampling. It is AC coupled on the input and output and has a fifty ohm output impedance. The typical output level is around +10 dBm, or about two volts, peak-to-peak.

This output is intended for direct digital sampling by a very high speed ADC. Unfortunately there is no suitable ADC on the market that can sample at a high enough speed to digitize the 60

MHz IF without aliasing. It is expected that such an ADC will be developed in the future and may be incorporated into the system to make use of the IF sample output. Until then the IF sample output can be used for any other purpose, such as a second monitor.

4.8 Calibration Switch

The most important signal path from the three way splitter is for the phase detector section. Out of the splitter the signal is amplified 12 decibels by a MAN-1HLN and is AC coupled. The MAN-1HLN is used since the signal must be at a level of about +10 dBm, which is well below the maximum output of the MAN-1HLN but over the one decibel compression point of the NE5204.

An SPDT pin diode calibration switch is placed between the MAN-1HLN and the phase detector section. It is a Mini-Circuits TOSW-230, with integral TTL drivers. It normally routes the IF signal from the MAN-1HLN to the phase detector section, with a small insertion loss. For a DC offset calibration, a 49.9 ohm resistor is connected to the phase detector section input. The switch is controlled from the control board and all eight channel switches are switched in parallel. A computer interface is on the control board to drive the switches from an external TTL signal. This is described in section five.

The calibration switch is part of a calibration system that is used to null out the DC offsets on the I and Q outputs. It will be implemented following the integration of the receiver into the EARS and the integration of the new data acquisition system, scheduled for December 1993.

4.9 Quadrature Phase Detector

This section produces the I and Q signals from the 60 MHz IF and reference signals. It uses four MCL parts, in the same way that the Zero IF and the old SAMPAR receivers do. The MCL devices used are;

TSC-2-1	two way 0 degree power splitter
PSCQ-2-70	two way 90 degree power splitter
MPD-1	phase detector (two)

The IF signal from the calibration switch goes to the TSC-2-1 splitter, at an ideal level of +10.5 dBm. It is split into two equal signals, with a loss of about 3.5 decibels. The signals each feed an MPD-1 phase detector.

The PSCQ-2-70 90 degree power splitter requires a 60 MHz reference at a level of about +10.5 dBm. This is provided by the frequency generation circuit, or exciter, located on the platform. The level of the reference input from the exciter is unknown but will probably be around 0 dBm. This signal is split into eight and amplified on the control board. The amplified reference is routed to each channel board using coaxial lines and is AC coupled.

The reference signal is amplified 12 decibels by a MAN-1HLN, therefore the optimum reference input level to the board is -1.5 dBm. The zero degree output of the PSCQ-2-70 feeds one of the MPD-1 phase detectors, while the 90 degree output feeds the other MPD-1. The MPD-1 that uses the zero degree reference signal outputs the I, or in-phase signal. The MPD-1 that uses the 90 degree reference signal outputs the Q, or quadrature phase signal. The outputs of the phase detectors are filtered with a simple RC low pass filter with a cutoff of about 15 MHz. This is to reduce the higher frequency components generated by the mixing action of the phase detectors.

4.10 First Baseband Gain Stage

The I, Q or offset video output signals must be amplified to a particular level to drive the data acquisition system to its full range. The minimum output of the MPD-1, with +7 dBm inputs, is specified at 750 millivolts. This is theoretical and in practice this level is seldom achieved. A more realistic output of 500 mV will be used for the gain calculations. If the old data acquisition systems are used to digitize the outputs, the maximum output voltage must be 5 VDC. Therefore the overall baseband voltage gain should be 5/0.5=10. The overall gain requirement for the new data acquisition system will be between 1 and 2 because of the smaller ADC voltage range.

With a possible overall gain requirement of 10, a distribution of the gain over two or three stages is recommended. Considering the gain of the active low pass filter and output driver described in following sections, a first gain stage before the low pass filter is useful. An AD846, described in the next section, is used in a non-inverting configuration to supply the gain and act as a buffer between the RC low pass filter and the active low pass filter section. A gain of 1 to 3 is suitable for this amplifier. If the feedback resistor is 1.2 KΩ and the resistor to ground is 1 KΩ a gain of 2.2 is produced. This can easily be changed by changing the value of the feedback resistor. This resistor can be anywhere in the range of 1 KΩ to about 10 KΩ without seriously affecting the performance of the AD846. A load resistor of 1 KΩ is used on the output.

When the new data acquisition system is integrated, a lower overall gain is required. The new ADC voltage range will be about +/-1 volt. If the MPD-1 output is 500 mV then a gain of only 2 is needed. Three gain stages are no longer necessary. The gain, noise and DC offset can be reduced by removing the first gain stage from the circuit. This can be done by soldering a jumper between the input (pin 3) and output (pin 6) of the AD846. The power supply lines should then be disabled to electrically remove the

AD846 from the circuit. The 1 KΩ output load resistor is also not needed. The alternative to removing the AD846 from the circuit is to adjust the resistors to make it a voltage follower. This is not recommended since a feedback resistor value of less than 1 kΩ may cause instability.

4.11 Low Pass Filters

Low pass filters are used to reduce the noise in the I and Q signals. The filter cutoff frequency is selected according to the pulse width used. A 'rule of thumb' is that the cutoff frequency should be the inverse of the pulse width. For example, a pulse width of 200 nanoseconds should have a filter with a 3 decibel cutoff frequency of no less than five megahertz.

It is not practical to have one low pass filter for each anticipated pulse width. The SLC system could receive radar returns with pulse widths of 200 nS, 500 nS, 800 nS, 1000 ns or 2000 nS. A design compromise is to have two filters with cutoffs of about one and five megahertz, such as in the Zero IF. The 5 MHz cutoff frequency filter is useful for the 200 nS, 500 nS and 800 nS pulse widths. The one megahertz cutoff frequency filter is good for the 1 µS and 2 µS pulse widths.

Active low pass filters are more suitable than passive filters since they provide gain and isolation. It is also easier to switch an active low pass filter between different corner frequencies. The order of a low pass filter controls the rate of attenuation outside the passband. Higher orders produce greater rates of attenuation, although they become increasingly complex and difficult to design as the order increases. The particular application governs which order to use. For filtering of the I and Q outputs a second order filter design is adequate. This requires a single operational amplifier. Each time the order is increased by two, another op-amp is required. For example a sixth order filter requires three op-amps.

There are many different configurations of active low pass filters, each with different characteristics. The most common low pass filter is the Butterworth. It is a general purpose compromise filter. All filters add phase shift to the signals passing through them. In order to preserve a pulse shape, a filter must add phase shift which is directly proportional to frequency. This will not cause phase distortion and will simply delay the pulse in time. This is a constant group delay filter.

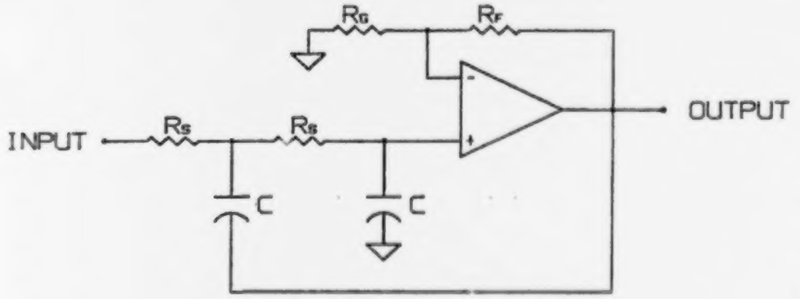
The only filter type with a constant group delay is the Bessel filter. It will cause a rise time that is inversely related to the corner frequency and will not cause ringing. The disadvantage to a Bessel filter is a slow roll-off near the corner frequency, although above twice the corner frequency the rolloff approaches the same slope as the Butterworth, at -12 dB per octave. The absolute constant delay time through the Bessel filter is not as important as the group delay variation over the filter bandwidth. The lower the group delay tolerance, the better the pulse response of the filter.

It is beyond the scope of this report to present a discussion of active filter configurations. A valuable reference that was used to design the low pass filters is the "Active-Filter Cookbook" (AFC) by Don Lancaster. It presents several low pass configurations. The one that was used is called the equal component value Sallen-Key circuit. It is a derivative of the second order Sallen-Key low pass filter and is shown in Figure Five. The two capacitors are identical in value and the two in-line resistors, R_S, are identical in value. The feedback resistor, R_F, must be 2-d times larger than the resistor to ground, R_G. The 'd' is termed the damping factor and controls the response. For a Bessel filter, d=1.732. Therefore resistor R_F must be 2-1.732= 0.268 times the value of R_G. The gain is fixed at 3-d=1.268= 2.1 dB.

A market survey of suitable op-amps to use for the low pass filter was made. Several possible op-amps were found and the one chosen was the AD846 precision current-feedback op-amp, by Analog Devices. It is relatively inexpensive and has good specifications. The manufacturer's specifications can be found in Appendix A. The key specifications are; input voltage noise 2 nV/√Hz, full power bandwidth 6.8 MHz at 20 V p-p, slew rate 450 V/µS, 10 V step settling time 80 nS to 0.1%, input offset voltage 75 µV.

A particular design procedure was used from the AFC. Components are given for a one kilohertz 3 dB corner frequency. In order to change the cutoff frequency the components need to be scaled linearly up or down. Halving the values of the in-line resistors doubles the cutoff frequency, also halving the values of the capacitors doubles the cutoff frequency. In order to keep the component values reasonable it was necessary to scale each one a certain amount. The new 3 dB cutoff frequencies desired are about 1.5 MHz and 7.7 MHz. These will produce an attenuation of about one decibel at 1 MHz and 5 MHz.

For a 1.5 MHz corner frequency the scale factor is 1500, starting with the 1 kHz corner frequency components. This scaling should be divided between the resistors and capacitors to keep their values reasonable. It is also important to keep the resistance to ground seen from the inverting and non-inverting inputs equal to keep the offset voltage to a minimum. The feedback resistor should be kept low so that the upper frequency limit of the amplifier is not compromised. The higher the feedback resistor above 1 kΩ, the lower the bandwidth. After many iterations, suitable component values were selected, considering component tolerances and available standard values. The in-line resistors



FOR A BESSEL FILTER, $d=1.732$ $R_F=(2-1.732)R_G=0.268R_G$

FOR A 1KHz -3dB FREQUENCY, $C=0.016\mu F$, $R_S=7.870\ \Omega$ AND $R_G=39.2K\Omega$

TO SCALE FREQUENCY UP, REDUCE THE CAPACITOR AND R_S VALUES, SINCE

$$F_c \propto \frac{1}{C} \text{ AND } F_c \propto \frac{1}{R_S}$$

Figure 5

EQUAL COMPONENT VALUE SALLEN-KEY LOW PASS BESSEL FILTER were calculated to be 390 ohms, the feedback resistor is 1000 ohms and the resistor to ground is 3.6 kΩ. The capacitors are 220 pF.

A similar iterative procedure was used to determine the 7.7 MHz corner frequency components. The components determined for the 1.5 MHz corner frequency were scaled by a factor of 5.13. It was decided to change just the capacitor values and to keep the resistors the same. The capacitors were calculated to be 47 pF. Therefore, in order to switch between the two cutoff frequencies it is only necessary to change the two capacitor values. This can be done with a relay. A search was made for a small printed circuit board mount relay with a low parasitic reactance. Capacitors connected in parallel are additive, so it was decided to use a dual SPST type relay to change the capacitor values. With the relay contacts open the 47 pF capacitors would be in the circuit, producing a 3 dB corner frequency of 6.9 MHz. Combining these in parallel with 180 pF capacitors produces an equivalent value of 227 pF, yielding a 3 dB corner frequency of 1.4 MHz.

The relay chosen to switch filter frequencies is the Potter and Brumfield JWD-171-25 plastic DIP package relay. It is inexpensive and small, with a dual SPST configuration (2FormA). All the eight channel filters are switched at the same time, via a common control line. It is not necessary to do this under computer control, so a simple toggle switch is used to control the relays. It is mounted on the control board front plate.

A suitable load resistor at the output of the low pass filter op amp was determined to be 820 ohms. In order to allow for a monitor point, this resistor is divided into two series resistors. A tap at one tenth the voltage output is used, so the resistors are 732 ohms and 82.5 ohms, as shown in the schematic. The monitor points are brought out to BNC connectors on the front panel for continuous operational monitoring. They are meant for the high impedance input of an oscilloscope.

4.12 Output Amplifier Line Drivers

The I and Q signals must be amplified to the appropriate levels for the data acquisition system, via 50 ohm coaxial lines. The output amplifiers and drivers perform this task. A suitable amplifier must have certain minimum specifications. Its noise output voltage should be less than an equivalent one half bit change in the ADC. It must have sufficient current drive for the maximum ADC range and bandwidth. A market survey was conducted to find a suitable device at a reasonable price. The Analog Devices AD842JN wideband high output current op amp was chosen. Its main specifications are; input voltage noise 9 nV/√Hz, output current 100 mA minimum, full power bandwidth 6.0 MHz for 20 V p-p, settling time 80 nS to 0.1% for 10 V step, slew rate 375 V/µS. To be unconditionally stable, the minimum recommended gain for the AD842 is two.

It is planned to use a twelve bit ADC in the new data acquisition system, with a range of about +/-1 volt. This gives a least significant bit (LSB) voltage of 488.4 µV. The output amplifier noise voltage should therefore be less than 244 µV. For the AD842, using a bandwidth of 6 MHz, the equivalent input noise voltage is 62 µVpp. This is translated to the output by multiplying it by the gain. A maximum gain of 3.9 can be used and still keep the noise to less than one half the LSB.

Considering a gain range of 2 to 3.9, resistance values were chosen, using the AD842 in a non-inverting configuration. The gain is variable using a 2 KΩ potentiometer in series with the 820 ohm feedback resistor. The resistor to ground is also 820 ohms. This combination allows a gain range of from 2 to 3.4.

The three op amps used in the I or Q baseband chain will generate a DC offset. The AD842 has a provision for nulling out a DC offset with a 10 kΩ potentiometer to the VCC rail. This is used to give a DC offset of less than one LSB on the I and Q outputs. Adjusting the DC offset pin of the AD842 will correct the offsets of all three op amps in the baseband chain. The AD842 can drive up to 20 pF without performance degradation and up to 100 pF without instability. A small value of capacitance is used at the output of the AD842 to decrease the noise above 10 MHz. A value of 47 pF is used as a first approximation. This value may be changed depending on the actual load capacitance in the coaxial cables and the data acquisition system.

4.13 Offset Video Output

An offset video output is provided. Its purpose is to enable an option for sampling at a bandwidth between the 60 MHz and the baseband video. Its bandwidth is approximately 5 MHz, between 1 and 6 MHz. The signal for the offset video output is taken from the output of the I section low pass filter, after the monitor resistors. The low pass filter must be in the 7 MHz corner frequency position to use the offset video section.

The offset video can be considered a second down converter. It has the advantage of a well defined bandwidth and the offset center frequency can be adjusted for system testing purposes. The bandwidth is limited to over 1 MHz by a simple RC high pass filter. The 3 dB corner frequency of the high pass filter should be about 600 kHz so the passband is not too attenuated. The resistance of this filter is the 820 ohm load of the low pass filter, so the capacitor should be about 330 pF to give the 600 kHz -3 dB corner frequency. An inductor could be added to make an LC high pass filter, if required. This would double the attenuation rolloff rate under 500 kHz which would result in slightly less noise.

The output driver is similar in design to the driver for the I and Q outputs. The new data acquisition system voltage range is less than +/-2 volts, so the drive current requirements are much less. Analog devices recommends using a 50 ohm resistor in series with the output when driving a nominal 50 ohm load over a 50 ohm coaxial line. This is to damp any stray transient signals that may be caused by impedance mismatches between the line and the load. This series resistor will drop the output voltage capability by half, an advantage for the offset video output.

An alternative to using the series 50 Ω resistor is to use a T-pad attenuator. This is useful if the overall gain is too high and the signal level must be attenuated. Setting the feedback potentiometer to zero will yield a gain of one, including the 50 Ω series resistor. Similar to the I and Q driver outputs, a 47 pF capacitor to ground is used to reduce very high frequency noise.

The offset video output is AC coupled to eliminate any DC offset and reduce the low frequency noise. A capacitor is in series with the final output line, after the 50 ohm series resistor, for the AC coupling. It acts as a high pass filter. A 6.8 nF capacitor is used in order to give a 500 kHz corner frequency.

4.14 Power Supplies and Distribution

The entire receiver requires five separate voltages; +15 VDC, -15 VDC, +12 VDC, -12 VDC, +5 VDC. A separate +/-15 VDC linear power supply should be used. The other voltages are derived from the +/-15 VDC using linear regulators. The regulators are located on each of the nine boards in the rack enclosure. Each channel board has three regulators and the control board two regulators. This distribution of power supplies improves the isolation between boards and reduces the number of power lines required to go to each board. A three position terminal strip is located on the backplane to accept the lines from the main external supply.

There are 16 active devices on each channel receiver board. They require +12 VDC, +5 VDC and -12 VDC. The following table details the supply voltages and currents required for each device. The current requirements are absolute maximums. Normally the current drawn will be much less than these values.

DEVICE PART NO.	SUPPLY VOLTAGE	MAX. CURRENT DRAW (mA)	NUMBER ON BOARD	TOTAL MAXIMUM CURRENT DRAW (mA)
MAN-1HLN	+12	70	5	350
NE5204	+12	35	2	70
AD846	+12	32	4	128
	-12	32	4	128
AD842	+12	115	3	345
	-12	115	3	345
DA0857	+5	5	1	5
TOSW-230	+5	10	1	10

Therefore each board requires +12 VDC @ 893 mA, +5 VDC @ 15 mA and -12 VDC @ 473 mA. These current requirements are met using a standard LM7812CT for the +12 VDC and an LM7912CT for the -12 VDC. These regulators are in TO-220 packages and can output over one ampere with a heat sink. Wakefield 270-AB heat sinks are used for each of these regulators. The current required from the +5 VDC supply is very low. An LM340LAH regulator in a TO-39 metal can package regulates the +5 VDC from the +12 VDC rail. This device can supply up to 100 mA without a heat sink.

Translating each voltage current requirement back to the +15 VDC and -15 VDC main supplies, and considering the power used by the regulators, the main current requirements can be determined. Each board requires +15 VDC @ 731 mA and -15 VDC @ 385 mA.

The control board has nine active devices on it. They require +15 VDC, +12 VDC, +5 VDC and -15 VDC. The table below details the maximum currents required by each device.

DEVICE PART NO.	SUPPLY VOLTAGE	MAX. CURRENT DRAW (mA)	NUMBER ON BOARD	TOTAL MAXIMUM CURRENT DRAW (mA)
MAN-1HLN	+12	70	1	70
74ALS138	+5	10	1	10
74ALS373	+5	112	3	336
AD395	+15	22	2	44
	-15	28	2	56
AD2701	-15	14	1	14
TOSW-230	+5	10	1	10

Therefore the control board requires +15 VDC @ 44 mA, +12 VDC @ 70 mA, +5 VDC @ 356 mA and -15 VDC @ 70 mA. Standard LM7812CT and LM7805CT regulators are used. The LM7805CT input is +12 VDC and both regulators use 270-AB heat sinks. The main supply current requirements are +15 VDC @ 233 mA and -15 VDC @ 70 mA.

Adding the main current requirements for the eight channel receiver boards and the control board, the main power supply must be capable of +15 VDC @ 6.08 A and -15 VDC @ 3.16 A. It is recommended that linear, rather than switching supplies be used to keep the noise on the supply lines to a minimum. Two possible supplies that can be used are the Lambda NNS50-15 for the -15 VDC supply and the Lambda LNS-W-15 for the +15 VDC supply. The two main linear power supplies should be mounted in a separate subrack.

5.0 CONTROL BOARD

There are eight identical receiver boards mounted in the 6U height card cage. There is also a ninth board for the control circuits. This board contains three distinct sections, two digital and one analogue. The analogue section is for the IF reference, including amplification, filtering and splitting.

One of the digital sections is for individual computer control of the eight channel phase shifters. The other section is for parallel control of all eight digital attenuators.

5.1 IF Reference Circuit

The nominal 60 MHz IF reference signal is produced by the TWTA exciter unit, located on the front end platform. An RG58 coaxial cable brings this signal to a connector on the rear of the control board. The signal is processed and eight identical reference signals are output to each channel.

5.1.1 Gain Stage and Bandpass Filter

A three decibel attenuator T-pad can be used to provide a 50 ohm impedance and to reduce reflections caused by mismatches through the cables and connectors. It is provided as an option and can be bypassed by soldering the coaxial cable directly to the next device.

The gain stage is a MAN-1HLN. It provides a fixed 12 decibel gain and is configured exactly the same as the MAN-1HLN devices used in the eight channels. It is AC coupled with a one nanofarad capacitor.

After the gain stage is a 60 MHz bandpass filter. This is the same design used in the eight channel receiver circuits. It has a three decibel bandwidth of 20 MHz, from 50 MHz to 70 MHz. It will therefore allow the IF reference to be changed from its nominal 60 MHz value. This accommodates the requirements of the offset video section for an offset IF reference.

5.1.2 Reference Monitor

A Mini Circuits TDC-10-1 directional coupler is used as a monitor port. It outputs a monitor signal which is 10 decibels down from the input. This is brought out to a BNC connector on the front panel of the control board via a coaxial cable. The monitor output has an impedance of 50 ohms. The TDC-10-1 causes a main line insertion loss of about 1.1 decibels.

5.1.3 Calibration Switch

A Mini Circuits TOSW-230 SPDT pin diode switch is used for computer controlled calibration of the DC offsets on the I and Q outputs. The switch control comes from an external computer through a 74ALS373 driver and 74S30 NAND gate located on the control board. For a calibration the eight switches are activated and the DC offsets are read on the I and Q outputs. The offset data is then used to correct the channel amplitude imbalances caused by the DC offsets.

5.1.4 Eight Way Splitter

A Mini Circuits PSC-8-1 eight way zero degree splitter provides eight identical IF reference outputs. Each reference output is routed to one of the boards via RG188 coaxial cable. The signal goes through two connectors and then directly into the reference amplifiers on each board. The splitter causes a nominal insertion loss of 10 decibels. The eight splitter outputs are balanced within 2.5 degrees and 0.3 decibels.

The optimum IF reference level into the PSCQ-2-70 two way 90 degree splitters is +10.5 dBm. MAN-1HLN amplifiers with 12 decibel gains are used ahead of the splitters. The required nominal IF reference signal level at the output of the eight way splitter is therefore -1.5 dBm. Tracing back to the IF reference input at the rear of the control board, a nominal level of +2.0 dBm is required. This is increased to +5.0 dBm if the three decibel T-pad is used. Assuming a cable loss from the exciter of 2.5 decibels, a nominal IF reference level of +4.5 dBm is needed from the exciter. This is increased to +7.5 dBm if the three decibel T-pad is used. The actual required IF reference level will be adjusted in the exciter.

5.2 Phase Shifter Interface

A digital computer interface is used on the control board for individual control of the PP-902 phase shifters. Each phase shifter has an individual 12 bit digital-to-analogue (DAC) converter driving it. Rather than use eight individual integrated circuits, a device was found that combines four 12 bit DACs into one package. This is the AD395 from Analog Devices. Each DAC is addressable and latches hold the last digital value written to each DAC. Therefore the DAC outputs are held at whatever level corresponds to the last digital value written. The specifications for the AD395 can be found in Appendix A. The analogue phase shifter control signals are sent to the phase shifters via coaxial cables, in order to keep the signals clean.

Two 74ALS373 octal latches are used to drive the data inputs to the AD395s from the computer. A 74ALS138 3 to 8 line demultiplexer selects one of the eight DACs for loading using a three bit address input. A phase shift/attenuator control select bit from the computer is used to de-select all the DACs by forcing the eight 74ALS138 outputs high. This would be done once the phase shifters were all set to their desired values. When each DAC is de-selected by bringing its select bit high, it will latch and hold the last value written to it.

The AD395 devices require a stable voltage reference to set the output voltage range. For a unipolar output range of zero to +10 volts, a reference voltage of -10.00 volts is required. Therefore a zero digital input produces a zero voltage output. A full scale input of 4095 gives a full scale output of +9.9976 volts. An AD2701JD -10.000 volt precision voltage reference is used. It can supply 10 mA of current which is enough to drive the two AD395s. It requires no external components and has a temperature coefficient of 3 ppm per degree Celsius. The absolute value of the reference voltage is not as important as the stability of the reference.

5.3 Digital Attenuator Interface

The computer interface for the digital attenuators is relatively simple. All the attenuators are controlled in parallel by five TTL bits. A 74ALS373 octal latch is used to drive the eight attenuators. This latch is transparent to the control bits when the phase shift/attenuator control select bit (P15) is high. When this control bit is brought low the five attenuator control bits are latched. Another 74ALS373 is used to buffer the attenuator control bits from the computer. This buffer is always totally transparent and is never latched.

5.4 Computer Interface Requirements

A computer with a sixteen bit parallel TTL level interface is required to control the phase and attenuator levels in the receiver. There are also manual methods of controlling both the attenuation and phase. The computer must also control the position of the nine calibration switches. It will have an algorithm to quickly equalize the phase differences between the channels. It is recommended that the phases be adjusted immediately before a data collection is made.

The TTL interface bits are on a male DB-25 connector located at the back of the control board. Standard ribbon cable can be used between the computer and the receiver. A toggle switch on the front panel of the control board selects between manual or computer control of the phase shifters.

5.4.1 Parallel Interface Control Bits

The computer controls the phase shifters and attenuators through a 16 bit parallel interface, designated PARBIT0 to PARBIT15 on the control board schematic. PARBIT~~15~~12 is the phase shift/ attenuator control select bit. When PARBIT~~15~~12 is high the phase shifters are de-selected and bits PARBIT1 through PARBIT5 control the attenuators. PARBIT1 is the least significant bit for the attenuators and PARBIT5 is the attenuator MSB. If PARBIT~~15~~12 is high, anything on the PARBIT1 to PARBIT5 inputs is sent directly to the attenuator control lines through two 74ALS373 latches. When PARBIT~~15~~12 is brought low the second 74ALS373 is latched and the attenuator's control inputs are fixed. The table below indicates the attenuations produced for various values of PARBIT1 through PARBIT5, with PARBIT~~15~~12 high. The smallest attenuation step is 2 decibels and the greatest attenuation is 62 dB. If PARBIT~~15~~12 is high, PARBIT6 and PARBIT7 are in a don't care state. PARBIT8 through PARBIT14 should be held low to inhibit control of the calibration switches.

PARBIT #					
5	4	3	2	1	Attenuation (dB)
0	0	0	0	0	0
0	0	0	0	1	2
0	0	0	1	0	4
0	0	1	0	0	8
0	1	0	0	0	16
1	0	0	0	0	32
0	0	0	1	1	6
0	0	1	1	1	14
0	1	1	1	0	28
1	1	1	1	1	62

When PARBIT~~15~~ 12 is low the phase shifter DACs can be written to. Bits 0 through 11 are connected to the twelve bit DAC data inputs, with all zeroes producing a zero phase shift. Bits 12, 13 and 14 are used for selecting the individual DAC to be written to, according to the table below.

PARBIT #			AD395 output pin selected	Channel Number Controlled
~~14~~ 15	~~13~~ 14	~~12~~ 13		
0	0	0	U4-27	1
0	0	1	U4-24	2
0	1	0	U4-21	3
0	1	1	U4-18	4
1	0	0	U5-27	5
1	0	1	U5-24	6
1	1	0	U5-21	7
1	1	1	U5-18	8

The full scale output of the AD395s is from 0 to about +10 volts. This corresponds to a phase shift by the PP-902 of zero to about 205 degrees. There is a particular combination of bits that will cause the nine calibration switches to switch to calibration mode. A 74S30 eight input NAND gate uses the upper eight parallel port bits, PARBIT8 to PARBIT15, as inputs. Only when these eight bits are all brought high will the output of the 74S30 go low, driving the switches to a calibration state. This condition also selects the attenuators for control and de-selects the phase shift interface. The control computer should not cause all the upper eight bits to go high unless a calibration is desired. Setting the upper eight bits all high would not normally occur with properly designed control software.

5.4.2 Computer Interface Timing Requirements

There are particular timing requirements for the computer control of the phase shifters and attenuators. The timing for the attenuators is simple and depends mainly on the DA0857 devices. They are of gallium arsenide construction and therefore have a high switching speed of 50 nanoseconds maximum and a typical rise/fall time of 12 nanoseconds at the RF output. The maximum rise/fall time is not specified. The switching delay time through two 74ALS373 latches is 16 nS. The time required from a control input change to an IF attenuation change is therefore 16+50+12= 78nS. It is recommended that a minimum time of 200 nanoseconds be allowed to switch the attenuators. This allows for line lengths and component tolerances.

The timing for the phase shifter control is more complex, considering the timing of the 74ALS373, 74ALS138, AD395 and PP-902. To enable control of the phase shifters the PARBIT15 line must be held low. The delay time through the 74ALS373 and 74ALS138 is a total of 33 nanoseconds. There is no specification given by Synergy for the time to change from zero degrees to a full scale phase change. They do specify the maximum control frequency is 50 kilohertz. This implies it would take about 10 microseconds for a maximum phase change to be reflected in the RF output.

Figure Six is the timing diagram that applies to the phase shift control. Due to the different delays through the 74ALS138 and 74ALS373, there must be a data access time of 8 ns minimum. This is the time from the PARBIT12, 13 or 14 change to the PARBIT0 to PARBIT11 data change. The chip select on the AD395s must be held low for at least 380 nS. This is controlled by PARBIT12, 13 and 14. The data must remain valid for at least 16 nS after the chip select changes. The settling time of the AD395 to within one half an LSB is 15 microseconds maximum. Once the AD395 is settled it will take about 10 microseconds for the PP-902 to change the phase of the RF output. Therefore the delay from selecting the channel to change to actually changing its phase is 25 microseconds. Allow 30 microseconds to change the phase, including a safety factor. The time required to disable the phase change interface by a low to high transition of PARBIT15 is 29 nanoseconds. During a radar trial data collection PARBIT15 should be held high.

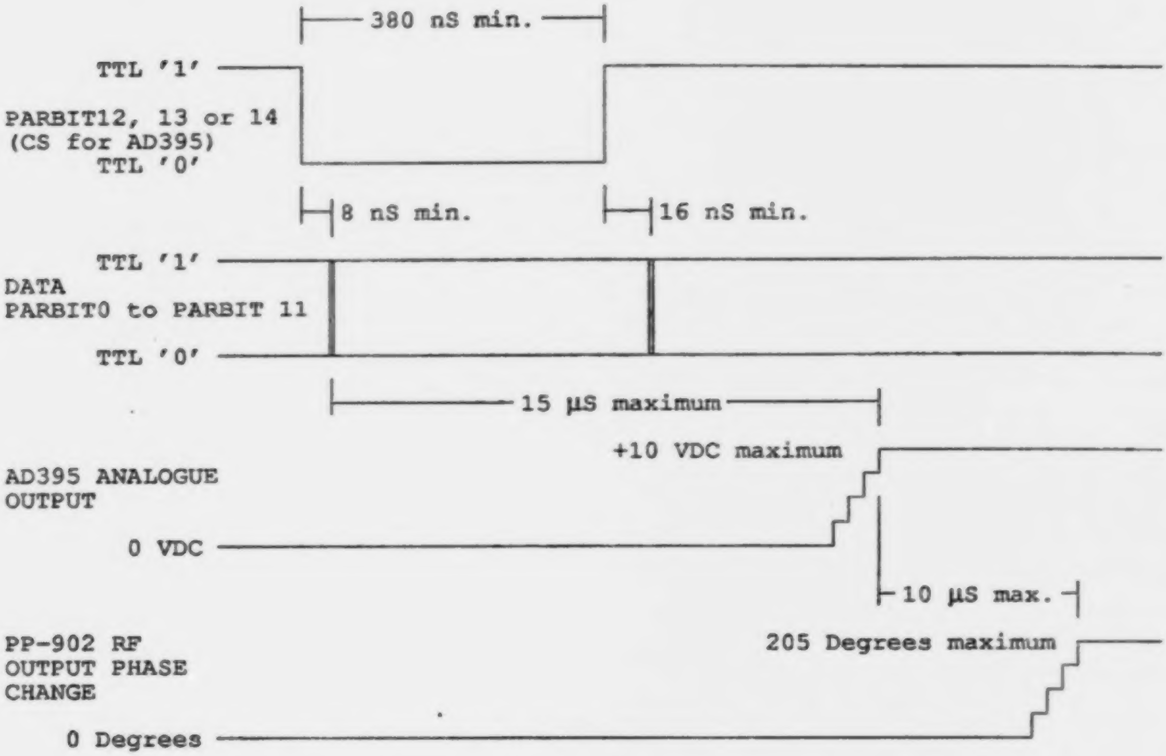

380 nS min.
TTL '1'
PARBIT12, 13 or 14
(CS for AD395)
TTL '0'
8 nS min.
16 nS min.
TTL '1'
DATA
PARBIT0 to PARBIT 11
TTL '0'
15 µS maximum
+10 VDC maximum
AD395 ANALOGUE
OUTPUT
0 VDC
10 µS max.
PP-902 RF
OUTPUT PHASE
CHANGE
205 Degrees maximum
0 Degrees

Figure 6

COMPUTER CONTROLLED PHASE SHIFT TIMING
(not to scale)

6.0 SIGNAL FLOW ANALYSIS

The design philosophy was to cause a change in the data acquisition ADC equal to only three to five LSBs for an IF input signal change from no signal to the minimum detectable IF signal. For signals near the maximum signal input level the digital attenuator is used to keep the signal within the ADC range. A noise only signal from the front end should ideally just cause the ADC LSB to change from 0 to 1. The dynamic range of the input signal is about 75 decibels. The IF receiver control should cause the full input dynamic range to use the full dynamic range of the data acquisition system.

The signal level from the IF input to each of the outputs can be traced. This is important to determine the limitations of the circuit and to ensure that each device operates in its linear region, above the noise floor but below saturation. The digital attenuator is used to limit the IF signal level when the IF input is above a certain point. For the purposes of this design description the circuit is divided into two sections. The first section is from the IF input to the phase detector section input. The second section covers the phase detector to the outputs.

6.1 IF Signal Flow Analysis

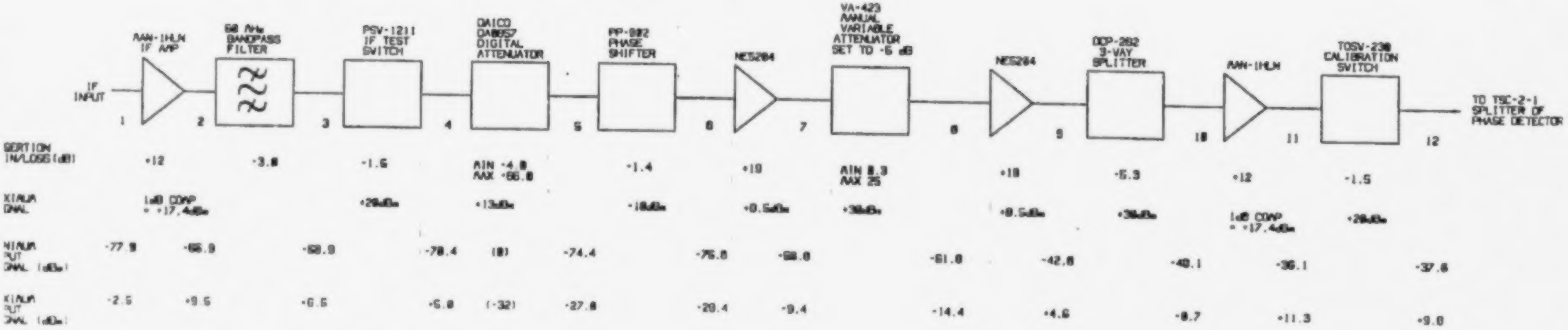
The 60 MHz IF signal level can be traced from the channel board IF input through to the phase detector section, where it is down converted. Each active or passive device in the IF chain has an effect on the signal. The passive devices cause an insertion loss and the active devices an insertion gain. Each device has an upper limit on its input signal level. For the active devices, there are two maximum signal input levels. A one decibel compression point is specified by the manufacturer and sometimes a damage point is also specified. It is important to keep the signal under the one decibel compression point to ensure linear operation.

Each active device contributes noise and distortion to the signal. For the active devices, the input signal noise should be greater than the noise floor of the active device. At the IF input, the noise floor is about -78 dBm. This is greater than the noise level of the MAN-1HLN first gain stage, as shown in section 4.1. As the IF signal is amplified, the noise is also amplified. The NE5204 has a noise figure of 6 decibels in a 50 Ω system. From section 4.4, with a bandwidth of 550 MHz, the noise floor of the NE5204 is -61.3 dBm, below the front end generated noise. The broadband noise is reduced by the 60 MHz bandpass filter.

Figure Seven is a block diagram of the IF chain. Each node between the devices is labelled, from 1 at the input to 12 at the phase detector input. Below each device are the specifications on its insertion gain or loss in decibels and its maximum signal in dBm. The maximum signal is the one decibel compression point for the active devices. The minimum input signal of -77.9 dBm is shown traced through the IF chain. The maximum input signal of -2.5 dBm is also calculated through the chain. The digital attenuator is not used for input signals below -30 dBm. The manual variable attenuator is set to 5 decibels for the calculations. This is a typical value and will vary from channel to channel.

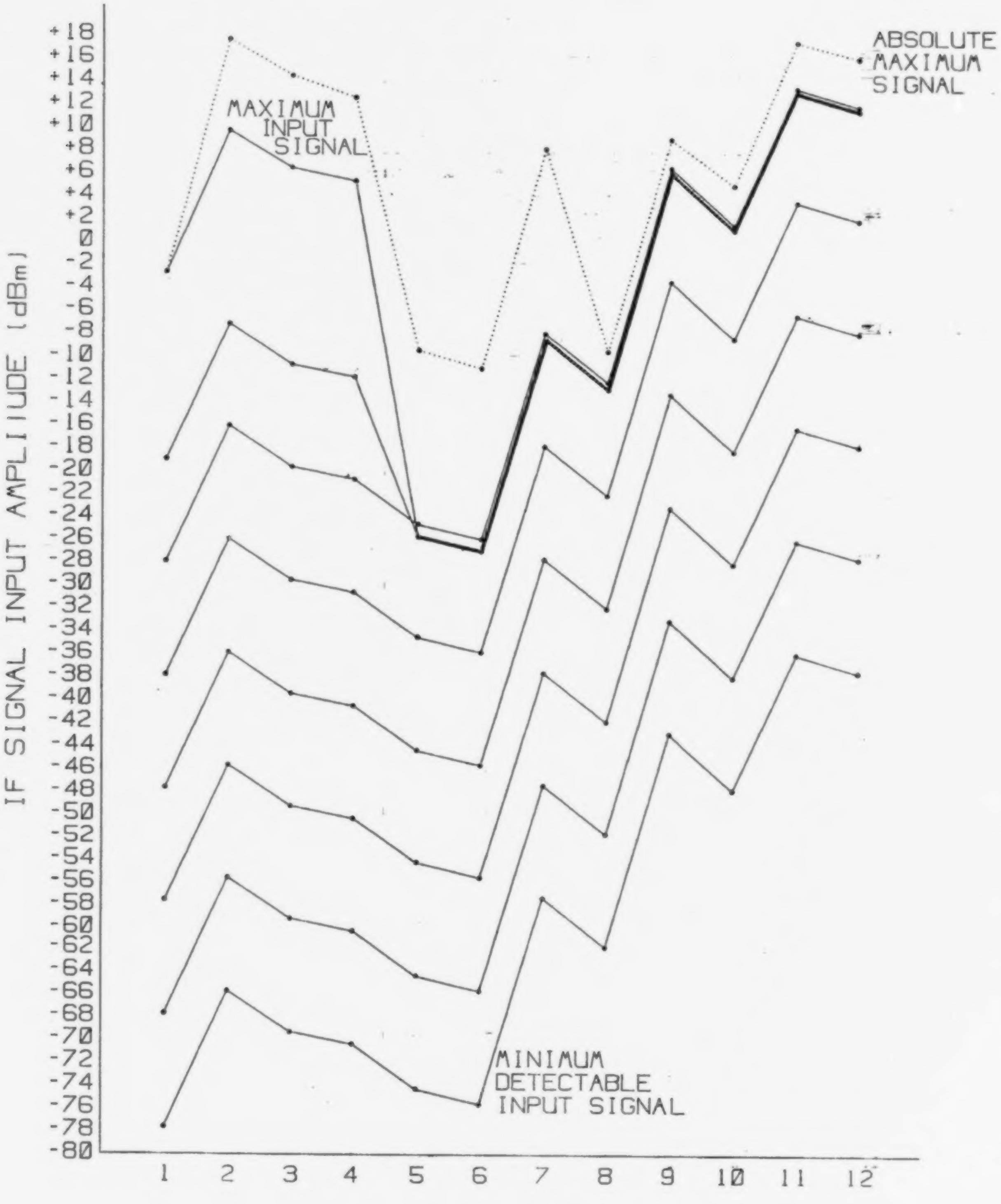
The ideal signal level into the phase detector section is +10.5 dBm. This produces the maximum undistorted phase detector output. This level cannot be reached until the input level is over -30 dBm. Figure Eight is a graphical representation of the signal amplitude numbers shown in Figure Seven and for six other intermediate levels. The numbers on the horizontal axis correspond to the circuit node numbers shown in Figure Seven. The absolute maximum signal through the chain is also shown. This is determined primarily by the one decibel compression points of the active devices. From Figure Eight it can be seen that the second NE5204, between nodes 8 and 9, is the first device to reach its one decibel

SIGNAL FLOW ANALYSIS


IF INPUT
AAN-1HLN IF AMP
60 MHz BANDPASS FILTER
PSV-1211 IF TEST SWITCH
DAICO DA0057 DIGITAL ATTENUATOR
PP-002 PHASE SHIFTER
NE5204
VA-423 MANUAL VARIABLE ATTENUATOR SET TO -6 dB
NE5204
DCP-202 3-WAY SPLITTER
AAN-1HLN
TOSV-230 CALIBRATION SWITCH
TO TSC-2-1 SPLITTER OF PHASE DETECTOR
1
2
3
4
5
6
7
8
9
10
11
12
SECTION GAIN/LOSS (dB)
+12
-3.0
-1.6
MIN -4.0 MAX -66.0
-1.4
+10
MIN 0.3 MAX 25
+10
-5.3
+12
-1.5
MAXIMUM SIGNAL
1dB COMP = +17.4dBm
+20dBm
+13dBm
+10dBm
+0.5dBm
+30dBm
+0.5dBm
+30dBm
1dB COMP = +17.4dBm
+20dBm
MINIMUM OUTPUT SIGNAL (dBm)
-77.9
-65.9
-68.9
-70.4
(0)
-74.4
-75.8
-65.8
-61.8
-42.8
-40.1
-36.1
-37.8
MAXIMUM OUTPUT SIGNAL (dBm)
-2.5
+9.5
+6.5
+5.0
(-32)
-27.0
-20.4
-9.4
-14.4
+4.6
-0.7
+11.3
+9.8

IF CHAIN BLOCK DIAGRAM

FIGURE 7



IF CHAIN SIGNAL LEVELS

FIGURE 8

compression point as the signal is increased over the maximum input signal level. This limits the setting of the manual variable attenuator to no less than about one decibel.

Between the -30 dBm and -2.5 dBm signal levels the digital attenuator is set to produce a signal at the phase detector section input as close to +10.5 dBm as possible. The phase detector section can produce a useable output with a signal level no lower than about -40 dBm. The minimum detectable input signal will yield a phase detector input signal of about -38 dBm. At this level the signal to noise ratio is very low.

6.2 Baseband Signal Flow Analysis

There are three active devices in the circuit chain to produce the I, Q or offset video outputs from the phase detector section. The first two amplifiers are fixed in gain and the output driver amplifier is variable in gain. Figure Nine is a block diagram of the three devices and their voltage gain settings.

The specified maximum output of the MPD-1 phase detector is at least 750 millivolts. To determine the transfer function of the phase detector section, some data was recorded in an experimental setup. The four devices comprising the phase detector section were connected on a PC board. The reference input to the 90 degree splitter was set to +10 dBm. The phase of the 60 MHz IF input was varied using two phase shifters until the maximum Q output level was reached for any given IF input level. The IF input level was changed in steps with a variable attenuator from +10.5 dBm down to -44.5 dBm. The Q output was filtered and monitored with an oscilloscope set with a 20 MHz bandwidth limit. The loads on the MPD-1 phase detectors were 500 ohms. The table below shows the data that was recorded from this experiment.

RF Input (dBm)	Q Output (mV DC)	RF Input (dBm)	Q Output (mV DC)
10.5	520	-1.5	138
9.5	465	-4.5	98
8.5	420	-9.5	54
7.5	380	-14.5	31.5
6.5	340	-19.5	17.5
5.5	300	-24.5	9.75
4.5	270	-29.5	5.5
3.5	242	-34.5	3
2.5	218	-39.5	1.5
1.5	195	-44.5	0.75
0.5	173		

At levels below -30 dBm the noise and higher frequency components made an accurate reading difficult. At these low levels the quality of the output is poor. This data reveals the

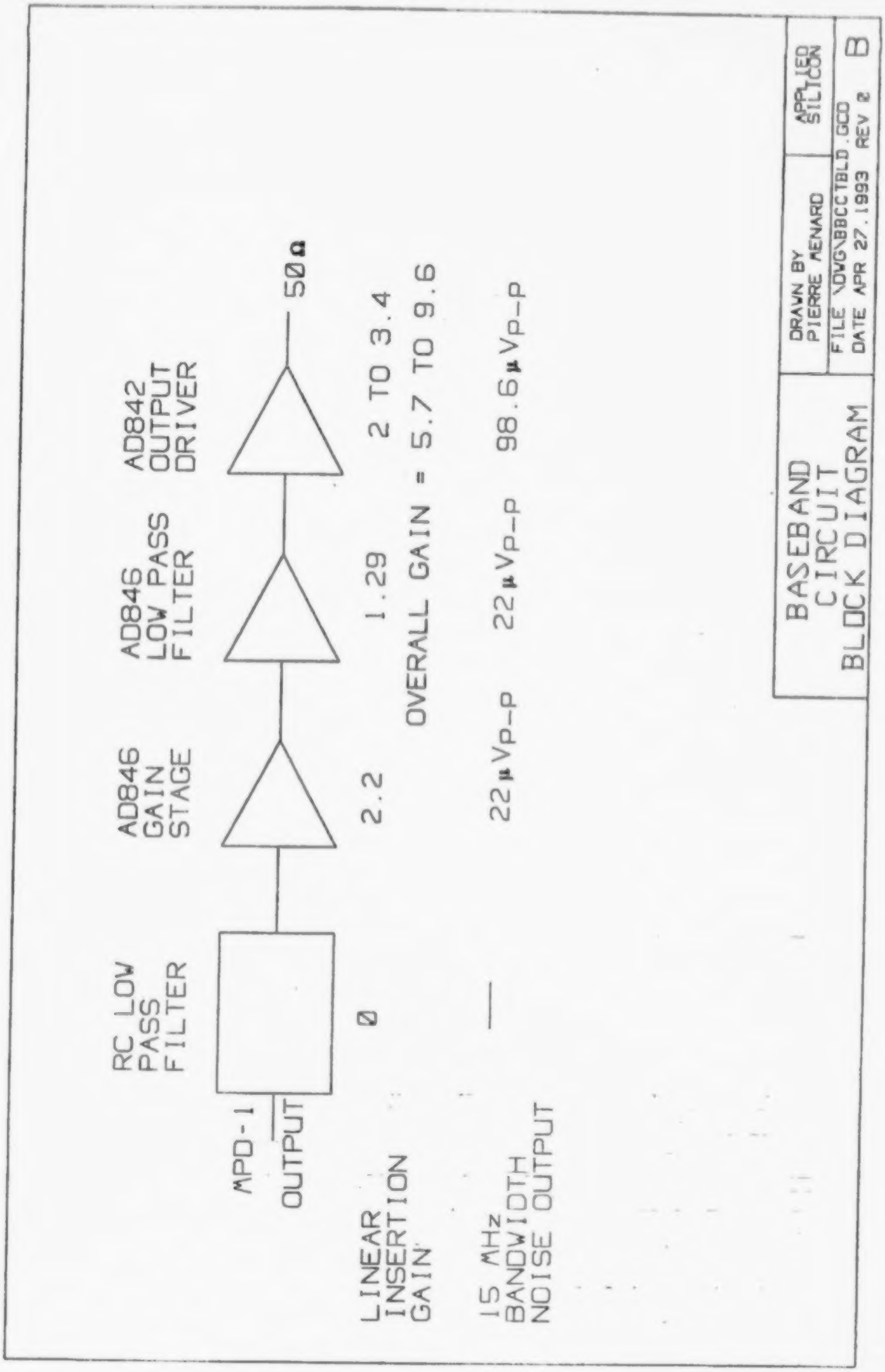

MPD-1 OUTPUT
RC LOW PASS FILTER
AD846 GAIN STAGE
AD846 LOW PASS FILTER
AD842 OUTPUT DRIVER
50Ω
LINEAR INSERTION GAIN
0
2.2
1.29
2 TO 3.4
OVERALL GAIN = 5.7 TO 9.6
15 MHz BANDWIDTH NOISE OUTPUT
—
22µVp-p
22µVp-p
22µVp-p
98.6µVp-p
BASEBAND CIRCUIT BLOCK DIAGRAM
DRAWN BY PIERRE MENARD
FILE \DWG\BBCCTBLD.GCD
DATE APR 27.1993
REV 2
APPLIED SILICON
B

FIGURE 9

characteristic curve of a phase detector. As the input level decreases the curve slope decreases, so for very low input levels the slope is very shallow. The maximum output was below that specified by Mini-Circuits. The level of the reference input was critical for getting the maximum output. If the reference level was slightly below the optimum level the output levels were significantly decreased, particularly for high signal input levels.

The gain of the active low pass filter is fixed at 1.29 due to its configuration as a Bessel filter. The first AD846 gain can be varied by changing the fixed feedback resistor. As a first calculation it has been set to 2.2, using a 1.2 KΩ feedback resistor. The gain of the AD842 output driver is variable with a potentiometer from 2 to 3.4. Multiplying the three gains together yields an overall gain of 5.7 to 9.6. With a phase detector output of 500 mV, the ADC input range is 2.85 VDC to 4.8 VDC. A phase detector of 750 mV produces and ADC input range of 4.3 VDC to 7.2 VDC.

The offset video output driver has a series 50 ohm resistor, as explained in section 4.13. This reduces the gain of the AD842 by half. Therefore the offset video output range is 1.425 VDC to 2.4 VDC with a 500 mV phase detector output and 2.14 VDC to 3.6 VDC with a 750 mV phase detector output. This is still a little high, so a resistor divider network can be placed at the AD842 input to reduce the level. This will be determined after testing the full prototype board.

The new data acquisition system will use a 12 bit ADC with a range of about +/-1 volt. This gives a resolution of .488 mV per LSB. From the experimental data and Figure Nine, a minimum input of -38 dBm to the phase detector section should produce an output of about 1.5 mVDC. An amplification of 2.85 produces 4.4 mV at the ADC input. This equates to 4.4 mV/.488 mV per bit= 9 bits. This is a little too high and can be remedied by reducing the overall gain in the offset video circuit. Either removing the first AD846 gain stage or introducing a resistor divider will reduce the gain sufficiently. A higher order high pass filter will also reduce the overall gain, with a further reduction in low frequency noise.

The existing data acquisition system has a 12 bit ADC range of 10 volts, yielding a resolution of 2.44 mV/bit. With a minimum phase detector output of 1.5 mV, the ADC will read from 3 to 6 bits. This meets the design goal stated at the start of section 6.0.

7.0 MECHANICAL DESCRIPTION

The SLC receiver is mounted in a standard 19 inch rack in the EARS portable laboratory. It obtains power from an external +/-15 VDC power supply located in the rack. The eight channel boards and the control board are mounted vertically in a subrack unit. This section describes the mechanical enclosure and all connections within the subrack and external connections to it.

7.1 Enclosure

The nine boards are contained in a Vero KM6-II Universal subrack. Each board is a standard double Eurocard 6U height and 240 mm depth size. The useable area on each board is 228 mm high by 214 mm. This is more than adequate since there is extra space on the channel board.

There are 84 hole positions (HP) across the width of the subrack. Since there are nine boards mounted in the subrack, the widest front panel that could be used is the 9 HP panel. This leaves a 3 HP width left over which can be covered with a blank panel. The plug-in units used are 9 HP wide with two rails. The optional left screens are in place to screen adjacent boards by covering the solder side of the boards. It may be necessary to increase the screening by installing custom made right screens over the component side. This could enclose each board except for the connector and adjustment access areas at the rear. Integrated system testing will be required to determine if co-channel interference is a problem. Using completely enclosed plug-in units presents a ventilation problem since the heat is trapped in the plug-in.

The optional ventilated EMC conversion kit is installed. This provides shielding on the top, bottom and rear of the subrack. The rear shield is a solid panel with screws at the top and hinges at the bottom. The top and bottom panels are ventilated. It is possible to obtain non-ventilated top and bottom panels to increase the shielding but the heat would be trapped in the subrack.

7.2 Connections and Cabling

There are nine coaxial inputs, 92 coaxial outputs and numerous power and control lines. This large number of connections presents interconnection difficulties. In order to minimize the problems and make board insertion or extraction easy it was decided to amalgamate control, power and coaxial connections into common shells. The KM6-II subrack is built to accommodate eurocards and their DIN 41612 type connectors. Two DIN 41612 connectors can be used on a 6U height eurocard. For the channel and control boards only one DIN 41612 shell connector is required in the lower connector position.

The channel board main connector is a DIN 41612 type M connector, manufactured by Harting Elecktronik. It contains 42 standard pin contacts and 6 coaxial contacts with a 50 ohm impedance. The coaxial connections use RG188 cable. The board connector is Harting part number 09031426901, with right angle pins. The coaxial cables from the board connectors are soldered directly to the board at the appropriate places. This yields the shortest track lengths on the board. Except for monitor and test points, the only coaxial connection not integrated into the DIN connector is the 60 MHz IF input. This uses a separate blind mate coaxial connector mounted on the rear upper section of the board.

The EARS system designates each main unit or major component with a number. The SLC receiver is unit number 33. All external connections to it are designated 33Jn where the n is an individual connector number. The eight 60 MHz IF inputs are externally designated as 33J1 to 33J8, for channels one to eight. The IF reference is 33J9. It goes to a separate blind mate coaxial connector on the upper rear section of the control board via a rear panel BNC bulkhead connector.

The rear hinged EMC panel is the bulkhead for mounting the signal output connectors. There are eight outputs for each of the I, Q, offset video and 60 MHz IF sample signals. A similar connection scheme to that used on the Zero IF receiver is used. There are four D shell connectors, each with eight coaxial lines in it. SMB type blind mate coaxial connectors are used in the 8W8 D shells. The four D shell connectors are mounted horizontally along the bottom of the hinged rear panel. Connector 33J10 is for the eight I outputs. Connector 33J11 is for the eight Q outputs. 33J12 is for the eight offset video outputs and 33J13 is for the eight IF sample outputs. Inside each D shell the connections are designated A1 to A8, corresponding to the channel number.

The eight IF inputs and the IF reference input are also brought through the rear panel using BNC bulkhead connectors. The inside of these connectors has an RG188 cable soldered directly to it. These cables go to each of the nine boards through the blind mate connections at the top rear of the boards.

The control board has eight IF reference outputs contained in an 8W8 D shell connector mounted on the rear upper section of the board. The eight coaxial connections lead to the DIN connectors on each channel board. Beside the 8W8 control board connector is a DB25 connector for all the external computer connections. This is for the connections to the computer parallel port to control the phase adjustments and digital attenuators.

There are numerous control connections from the control board to each of the eight channel boards. These are brought over the pin connections in the center of the DIN 41612 connectors. They are mostly TTL level signals and do not need coaxial lines. A small backplane is used for these lines. The +/-15 VDC power lines are also on the backplane to each board. A three position terminal strip on the backplane accepts the wires from the main outboard power supply.

The following series of tables detail the connections for the SLC receiver. They are divided into functional groups for the internal and external connections. Some explanations are needed for the abbreviations used in the tables.

Under the TYPE column, a 'BNC-F' refers to a BNC female bulkhead connector. The external part of this connector is a BNC female, while the internal part accepts the RG188 coaxial cable. M/A-COM clamp attachment bulkhead feedthrough BNC cable jack connector, part number 3204-7388-10, is suitable for this connector. The type designation 'MA-COM OSP' refers to a particular blind mate coaxial connector made by M/A-COM. The crimp attachment bulkhead feedthrough cable plug is part number 4533-7388-02. Its mate is the crimp attachment panel feedthrough cable jack, part number 4540-7388-02. These connectors are called OSP miniature blind mate connectors for flexible cable by M/A-COM.

RECEIVER CONNECTOR GENERAL DESCRIPTIONS

CONNECTOR DESIGNAT.	TYPE	LOCATION	DESCRIPTION
33J1	BNC-F	REAR PANEL	CHANNEL 1 IF INPUT
33J2	BNC-F	REAR PANEL	CHANNEL 2 IF INPUT
33J3	BNC-F	REAR PANEL	CHANNEL 3 IF INPUT
33J4	BNC-F	REAR PANEL	CHANNEL 4 IF INPUT
33J5	BNC-F	REAR PANEL	CHANNEL 5 IF INPUT
33J6	BNC-F	REAR PANEL	CHANNEL 6 IF INPUT
33J7	BNC-F	REAR PANEL	CHANNEL 7 IF INPUT
33J8	BNC-F	REAR PANEL	CHANNEL 8 IF INPUT
33J9	BNC-F	REAR PANEL	IF REFERENCE INPUT
33J10	8W8 D	REAR PANEL	EIGHT I OUTPUTS
33J11	8W8 D	REAR PANEL	EIGHT Q OUTPUTS
33J12	8W8 D	REAR PANEL	EIGHT OFFSET VIDEO
33J13	8W8 D	REAR PANEL	EIGHT IF SAMPLE OUT
33J14	MA-COM OSP	TOP REAR CH. 1 BOARD	CHANNEL 1 IF INPUT
33J15	MA-COM OSP	TOP REAR CH. 2 BOARD	CHANNEL 2 IF INPUT
33J16	MA-COM OSP	TOP REAR CH. 3 BOARD	CHANNEL 3 IF INPUT
33J17	MA-COM OSP	TOP REAR CH. 4 BOARD	CHANNEL 4 IF INPUT
33J18	MA-COM OSP	TOP REAR CH. 5 BOARD	CHANNEL 5 IF INPUT
33J19	MA-COM OSP	TOP REAR CH. 6 BOARD	CHANNEL 6 IF INPUT
33J20	MA-COM OSP	TOP REAR CH. 7 BOARD	CHANNEL 7 IF INPUT
33J21	MA-COM OSP	TOP REAR CH. 8 BOARD	CHANNEL 8 IF INPUT
33J22	MA-COM OSP	TOP REAR CONT. BOARD	IF REFERENCE INPUT
33J23	DB-25 MALE	TOP REAR CONT. BOARD	COMPUTER CONTROL
33J24	8W8 D	TOP REAR CONT. BOARD	EIGHT IF REFERENCES
33J25	41612M 24+8	LOWER REAR REF. BOARD	8 PHASE ADJUSTS, PINS
33J26	41612M 42+6	LOWER REAR CH.1 BOARD	MULTIPLE COAX/PIN
33J27	41612M 42+6	LOWER REAR CH.2 BOARD	MULTIPLE COAX/PIN
33J28	41612M 42+6	LOWER REAR CH.3 BOARD	MULTIPLE COAX/PIN
33J29	41612M 42+6	LOWER REAR CH.4 BOARD	MULTIPLE COAX/PIN
33J30	41612M 42+6	LOWER REAR CH.5 BOARD	MULTIPLE COAX/PIN

33J31	41612M 42+6	LOWER REAR CH.6 BOARD	MULTIPLE COAX/PIN
33J32	41612M 42+6	LOWER REAR CH.7 BOARD	MULTIPLE COAX/PIN
33J33	41612M 42+6	LOWER REAR CH.8 BOARD	MULTIPLE COAX/PIN
33J34	TERM. STRIP	ON BACKPLANE	MAIN POWER INPUT
33J35	BNC-F	CONTROL BOARD FRONT	IF REF. MONITOR
33J36	BNC-F	CHANNEL 1 FRONT PANEL	IF TEST SIGNAL IN
33J37	BNC-F	CHANNEL 1 FRONT PANEL	I MONITOR OUTPUT
33J38	BNC-F	CHANNEL 1 FRONT PANEL	Q MONITOR OUTPUT
33J39	BNC-F	CHANNEL 1 FRONT PANEL	IF MONITOR OUTPUT
33J40	BNC-F	CHANNEL 2 FRONT PANEL	IF TEST SIGNAL IN
33J41	BNC-F	CHANNEL 2 FRONT PANEL	I MONITOR OUTPUT
33J42	BNC-F	CHANNEL 2 FRONT PANEL	Q MONITOR OUTPUT
33J43	BNC-F	CHANNEL 2 FRONT PANEL	IF MONITOR OUTPUT
33J44	BNC-F	CHANNEL 3 FRONT PANEL	IF TEST SIGNAL IN
33J45	BNC-F	CHANNEL 3 FRONT PANEL	I MONITOR OUTPUT
33J46	BNC-F	CHANNEL 3 FRONT PANEL	Q MONITOR OUTPUT
33J47	BNC-F	CHANNEL 3 FRONT PANEL	IF MONITOR OUTPUT
33J48	BNC-F	CHANNEL 4 FRONT PANEL	IF TEST SIGNAL IN
33J49	BNC-F	CHANNEL 4 FRONT PANEL	I MONITOR OUTPUT
33J50	BNC-F	CHANNEL 4 FRONT PANEL	Q MONITOR OUTPUT
33J51	BNC-F	CHANNEL 4 FRONT PANEL	IF MONITOR OUTPUT
33J52	BNC-F	CHANNEL 5 FRONT PANEL	IF TEST SIGNAL IN
33J53	BNC-F	CHANNEL 5 FRONT PANEL	I MONITOR OUTPUT
33J54	BNC-F	CHANNEL 5 FRONT PANEL	Q MONITOR OUTPUT
33J55	BNC-F	CHANNEL 5 FRONT PANEL	IF MONITOR OUTPUT
33J56	BNC-F	CHANNEL 6 FRONT PANEL	IF TEST SIGNAL IN
33J57	BNC-F	CHANNEL 6 FRONT PANEL	I MONITOR OUTPUT
33J58	BNC-F	CHANNEL 6 FRONT PANEL	Q MONITOR OUTPUT
33J59	BNC-F	CHANNEL 6 FRONT PANEL	IF MONITOR OUTPUT
33J60	BNC-F	CHANNEL 7 FRONT PANEL	IF TEST SIGNAL IN
33J61	BNC-F	CHANNEL 7 FRONT PANEL	I MONITOR OUTPUT
33J62	BNC-F	CHANNEL 7 FRONT PANEL	Q MONITOR OUTPUT
33J63	BNC-F	CHANNEL 7 FRONT PANEL	IF MONITOR OUTPUT
33J64	BNC-F	CHANNEL 8 FRONT PANEL	IF TEST SIGNAL IN
33J65	BNC-F	CHANNEL 8 FRONT PANEL	I MONITOR OUTPUT
33J66	BNC-F	CHANNEL 8 FRONT PANEL	Q MONITOR OUTPUT
33J67	BNC-F	CHANNEL 8 FRONT PANEL	IF MONITOR OUTPUT

EXTERNAL IF AND REFERENCE INPUTS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J1	BNC-F	CHANNEL 1 IF INPUT	33J14
33J2	BNC-F	CHANNEL 2 IN INPUT	33J15
33J3	BNC-F	CHANNEL 3 IF INPUT	33J16
33J4	BNC-F	CHANNEL 4 IN INPUT	33J17
33J5	BNC-F	CHANNEL 5 IF INPUT	33J18
33J6	BNC-F	CHANNEL 6 IN INPUT	33J19
33J7	BNC-F	CHANNEL 7 IF INPUT	33J20
33J8	BNC-F	CHANNEL 8 IN INPUT	33J21
33J9	BNC-F	IF REFERENCE INPUT	33J22

REAR EXTERNAL SIGNAL OUTPUTS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J10-A1	8W8 D-SHELL	CHANNEL 1 I OUTPUT	33J26-5
33J10-A2	8W8 D-SHELL	CHANNEL 2 I OUTPUT	33J27-5
33J10-A3	8W8 D-SHELL	CHANNEL 3 I OUTPUT	33J28-5
33J10-A4	8W8 D-SHELL	CHANNEL 4 I OUTPUT	33J29-5
33J10-A5	8W8 D-SHELL	CHANNEL 5 I OUTPUT	33J30-5
33J10-A6	8W8 D-SHELL	CHANNEL 6 I OUTPUT	33J31-5
33J10-A7	8W8 D-SHELL	CHANNEL 7 I OUTPUT	33J32-5
33J10-A8	8W8 D-SHELL	CHANNEL 8 I OUTPUT	33J33-5
33J11-A1	8W8 D-SHELL	CHANNEL 1 Q OUTPUT	33J26-8
33J11-A2	8W8 D-SHELL	CHANNEL 2 Q OUTPUT	33J27-8
33J11-A3	8W8 D-SHELL	CHANNEL 3 Q OUTPUT	33J28-8
33J11-A4	8W8 D-SHELL	CHANNEL 4 Q OUTPUT	33J29-8
33J11-A5	8W8 D-SHELL	CHANNEL 5 Q OUTPUT	33J30-8
33J11-A6	8W8 D-SHELL	CHANNEL 6 Q OUTPUT	33J31-8
33J11-A7	8W8 D-SHELL	CHANNEL 7 Q OUTPUT	33J32-8
33J11-A8	8W8 D-SHELL	CHANNEL 8 Q OUTPUT	33J33-8
33J12-A1	8W8 D-SHELL	CHANNEL 1 OFFSET VIDEO OUTPUT	33J26-28
33J12-A2	8W8 D-SHELL	CHANNEL 2 OFFSET VIDEO OUTPUT	33J27-28
33J12-A3	8W8 D-SHELL	CHANNEL 3 OFFSET VIDEO OUTPUT	33J28-28
33J12-A4	8W8 D-SHELL	CHANNEL 4 OFFSET VIDEO OUTPUT	33J29-28
33J12-A5	8W8 D-SHELL	CHANNEL 5 OFFSET VIDEO OUTPUT	33J30-28
33J12-A6	8W8 D-SHELL	CHANNEL 6 OFFSET VIDEO OUTPUT	33J31-28
33J12-A7	8W8 D-SHELL	CHANNEL 7 OFFSET VIDEO OUTPUT	33J32-28
33J12-A8	8W8 D-SHELL	CHANNEL 8 OFFSET VIDEO OUTPUT	33J33-28
33J13-A1	8W8 D-SHELL	CHANNEL 1 IF SAMPLE OUTPUT	33J26-31
33J13-A2	8W8 D-SHELL	CHANNEL 2 IF SAMPLE OUTPUT	33J27-31
33J13-A3	8W8 D-SHELL	CHANNEL 3 IF SAMPLE OUTPUT	33J28-31
33J13-A4	8W8 D-SHELL	CHANNEL 4 IF SAMPLE OUTPUT	33J29-31
33J13-A5	8W8 D-SHELL	CHANNEL 5 IF SAMPLE OUTPUT	33J30-31
33J13-A6	8W8 D-SHELL	CHANNEL 6 IF SAMPLE OUTPUT	33J31-31
33J13-A7	8W8 D-SHELL	CHANNEL 7 IF SAMPLE OUTPUT	33J32-31
33J13-A8	8W8 D-SHELL	CHANNEL 8 IF SAMPLE OUTPUT	33J33-31

CHANNEL ONE BOARD CONNECTIONS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J14	MA-COM OSP	60 MHZ IF INPUT	33J1
33J26-2	41612M 42+6	60 MHZ REFERENCE INPUT	33J24-A1
33J26-5	41612M 42+6	I OUTPUT	33J10-A1
33J26-8	41612M 42+6	Q OUTPUT	33J11-A1
33J26-25	41612M 42+6	PHASE CONTROL VOLTAGE INPUT	33J25-2
33J26-28	41612M 42+6	OFFSET VIDEO OUTPUT	33J12-A1
33J26-31	41612M 42+6	IF SAMPLE OUTPUT	33J13-A1
33J26-10abc	41612M 42+6	+15 VDC BOARD POWER INPUT	33J34-1
33J26-11abc	41612M 42+6	GROUND	33J34-2
33J26-12abc	41612M 42+6	DIGITAL ATTEN. CONTROL LSB	33J25-14a
33J26-13abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 2	33J25-15a
33J26-14abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 3	33J25-16a
33J26-15abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 4	33J25-17a
33J26-16abc	41612M 42+6	DIGITAL ATTEN. CONTROL MSB	33J25-18a
33J26-17abc	41612m 42+6	LOW PASS FILTER CONTROL IN	33J25-14c
33J26-18abc	41612M 42+6	CALIBRATION SWITCH CONTR. IN	33J25-15c
33J26-19abc	41612M 42+6	PHASE ADJUST SOURCE CONTROL	33J25-16c
33J26-20abc	41612M 42+6	NORMAL/TEST IF SELECT HIGH	33J25-17c
33J26-21abc	41612M 42+6	NORMAL/TEST IF SELECT LOW	33J25-18c
33J26-22abc	41612M 42+6	GROUND	33J34-2
33J26-23abc	41612M 42+6	-15 VDC BOARD POWER INPUT	33J34-3
33J36	BNC-F	IF TEST SIGNAL INPUT, 50 Ω	ON BOARD
33J37	BNC-F	I MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J38	BNC-F	Q MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J39	BNC-F	IF MONITOR OUTPUT, 50 Ω	ON BOARD

CHANNEL TWO BOARD CONNECTIONS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J15	MA-COM OSP	60 MHZ IF INPUT	33J2
33J27-2	41612M 42+6	60 MHZ REFERENCE INPUT	33J24-A2
33J27-5	41612M 42+6	I OUTPUT	33J10-A2
33J27-8	41612M 42+6	Q OUTPUT	33J11-A2
33J27-25	41612M 42+6	PHASE CONTROL VOLTAGE INPUT	33J25-5
33J27-28	41612M 42+6	OFFSET VIDEO OUTPUT	33J12-A2
33J27-31	41612M 42+6	IF SAMPLE OUTPUT	33J13-A2
33J27-10abc	41612M 42+6	+15 VDC BOARD POWER INPUT	33J34-1
33J27-11abc	41612M 42+6	GROUND	33J34-2
33J27-12abc	41612M 42+6	DIGITAL ATTEN. CONTROL LSB	33J25-14a
33J27-13abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 2	33J25-15a
33J27-14abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 3	33J25-16a
33J27-15abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 4	33J25-17a
33J27-16abc	41612M 42+6	DIGITAL ATTEN. CONTROL MSB	33J25-18a
33J27-17abc	41612m 42+6	LOW PASS FILTER CONTROL IN	33J25-14c
33J27-18abc	41612M 42+6	CALIBRATION SWITCH CONTR. IN	33J25-15c
33J27-19abc	41612M 42+6	PHASE ADJUST SOURCE CONTROL	33J25-16c
33J27-20abc	41612M 42+6	NORMAL/TEST IF SELECT HIGH	33J25-17c
33J27-21abc	41612M 42+6	NORMAL/TEST IF SELECT LOW	33J25-18c
33J27-22abc	41612M 42+6	GROUND	33J34-2
33J27-23abc	41612M 42+6	-15 VDC BOARD POWER INPUT	33J34-3
33J40	BNC-F	IF TEST SIGNAL INPUT, 50 Ω	ON BOARD
33J41	BNC-F	I MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J42	BNC-F	Q MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J43	BNC-F	IF MONITOR OUTPUT, 50 Ω	ON BOARD

CHANNEL THREE BOARD CONNECTIONS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J16	MA-COM OSP	60 MHZ IF INPUT	33J3
33J28-2	41612M 42+6	60 MHZ REFERENCE INPUT	33J24-A3
33J28-5	41612M 42+6	I OUTPUT	33J10-A3
33J28-8	41612M 42+6	Q OUTPUT	33J11-A3
33J28-25	41612M 42+6	PHASE CONTROL VOLTAGE INPUT	33J25-8
33J28-28	41612M 42+6	OFFSET VIDEO OUTPUT	33J12-A3
33J28-31	41612M 42+6	IF SAMPLE OUTPUT	33J13-A3
33J28-10abc	41612M 42+6	+15 VDC BOARD POWER INPUT	33J34-1
33J28-11abc	41612M 42+6	GROUND	33J34-2
33J28-12abc	41612M 42+6	DIGITAL ATTEN. CONTROL LSB	33J25-14a
33J28-13abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 2	33J25-15a
33J28-14abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 3	33J25-16a
33J28-15abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 4	33J25-17a
33J28-16abc	41612M 42+6	DIGITAL ATTEN. CONTROL MSB	33J25-18a
33J28-17abc	41612m 42+6	LOW PASS FILTER CONTROL IN	33J25-14c
33J28-18abc	41612M 42+6	CALIBRATION SWITCH CONTR. IN	33J25-15c
33J28-19abc	41612M 42+6	PHASE ADJUST SOURCE CONTROL	33J25-16c
33J28-20abc	41612M 42+6	NORMAL/TEST IF SELECT HIGH	33J25-17c
33J28-21abc	41612M 42+6	NORMAL/TEST IF SELECT LOW	33J25-18c
33J28-22abc	41612M 42+6	GROUND	33J34-2
33J28-23abc	41612M 42+6	-15 VDC BOARD POWER INPUT	33J34-3
33J44	BNC-F	IF TEST SIGNAL INPUT, 50 Ω	ON BOARD
33J45	BNC-F	I MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J46	BNC-F	Q MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J47	BNC-F	IF MONITOR OUTPUT, 50 Ω	ON BOARD

CHANNEL FOUR BOARD CONNECTIONS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J17	MA-COM OSP	60 MHZ IF INPUT	33J4
33J29-2	41612M 42+6	60 MHZ REFERENCE INPUT	33J24-A4
33J29-5	41612M 42+6	I OUTPUT	33J10-A4
33J29-8	41612M 42+6	Q OUTPUT	33J11-A4
33J29-25	41612M 42+6	PHASE CONTROL VOLTAGE INPUT	33J25-11
33J29-28	41612M 42+6	OFFSET VIDEO OUTPUT	33J12-A4
33J29-31	41612M 42+6	IF SAMPLE OUTPUT	33J13-A4
33J29-10abc	41612M 42+6	+15 VDC BOARD POWER INPUT	33J34-1
33J29-11abc	41612M 42+6	GROUND	33J34-2
33J29-12abc	41612M 42+6	DIGITAL ATTEN. CONTROL LSB	33J25-14a
33J29-13abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 2	33J25-15a
33J29-14abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 3	33J25-16a
33J29-15abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 4	33J25-17a
33J29-16abc	41612M 42+6	DIGITAL ATTEN. CONTROL MSB	33J25-18a
33J29-17abc	41612m 42+6	LOW PASS FILTER CONTROL IN	33J25-14c
33J29-18abc	41612M 42+6	CALIBRATION SWITCH CONTR. IN	33J25-15c
33J29-19abc	41612M 42+6	PHASE ADJUST SOURCE CONTROL	33J25-16c
33J29-20abc	41612M 42+6	NORMAL/TEST IF SELECT HIGH	33J25-17c
33J29-21abc	41612M 42+6	NORMAL/TEST IF SELECT LOW	33J25-18c
33J29-22abc	41612M 42+6	GROUND	33J34-2
33J29-23abc	41612M 42+6	-15 VDC BOARD POWER INPUT	33J34-3
33J48	BNC-F	IF TEST SIGNAL INPUT, 50 Ω	ON BOARD
33J49	BNC-F	I MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J50	BNC-F	Q MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J51	BNC-F	IF MONITOR OUTPUT, 50 Ω	ON BOARD

CHANNEL FIVE BOARD CONNECTIONS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J18	MA-COM OSP	60 MHZ IF INPUT	33J5
33J30-2	41612M 42+6	60 MHZ REFERENCE INPUT	33J24-A5
33J30-5	41612M 42+6	I OUTPUT	33J10-A5
33J30-8	41612M 42+6	Q OUTPUT	33J11-A5
33J30-25	41612M 42+6	PHASE CONTROL VOLTAGE INPUT	33J25-22
33J30-28	41612M 42+6	OFFSET VIDEO OUTPUT	33J12-A5
33J30-31	41612M 42+6	IF SAMPLE OUTPUT	33J13-A5
33J30-10abc	41612M 42+6	+15 VDC BOARD POWER INPUT	33J34-1
33J30-11abc	41612M 42+6	GROUND	33J34-2
33J30-12abc	41612M 42+6	DIGITAL ATTEN. CONTROL LSB	33J25-14a
33J30-13abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 2	33J25-15a
33J30-14abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 3	33J25-16a
33J30-15abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 4	33J25-17a
33J30-16abc	41612M 42+6	DIGITAL ATTEN. CONTROL MSB	33J25-18a
33J30-17abc	41612m 42+6	LOW PASS FILTER CONTROL IN	33J25-14c
33J30-18abc	41612M 42+6	CALIBRATION SWITCH CONTR. IN	33J25-15c
33J30-19abc	41612M 42+6	PHASE ADJUST SOURCE CONTROL	33J25-16c
33J30-20abc	41612M 42+6	NORMAL/TEST IF SELECT HIGH	33J25-17c
33J30-21abc	41612M 42+6	NORMAL/TEST IF SELECT LOW	33J25-18c
33J30-22abc	41612M 42+6	GROUND	33J34-2
33J30-23abc	41612M 42+6	-15 VDC BOARD POWER INPUT	33J34-3
33J52	BNC-F	IF TEST SIGNAL INPUT, 50 Ω	ON BOARD
33J53	BNC-F	I MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J54	BNC-F	Q MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J55	BNC-F	IF MONITOR OUTPUT, 50 Ω	ON BOARD

CHANNEL SIX BOARD CONNECTIONS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J19	MA-COM OSP	60 MHZ IF INPUT	33J6
33J31-2	41612M 42+6	60 MHZ REFERENCE INPUT	33J24-A6
33J31-5	41612M 42+6	I OUTPUT	33J10-A6
33J31-8	41612M 42+6	Q OUTPUT	33J11-A6
33J31-25	41612M 42+6	PHASE CONTROL VOLTAGE INPUT	33J25-25
33J31-28	41612M 42+6	OFFSET VIDEO OUTPUT	33J12-A6
33J31-31	41612M 42+6	IF SAMPLE OUTPUT	33J13-A6
33J31-10abc	41612M 42+6	+15 VDC BOARD POWER INPUT	33J34-1
33J31-11abc	41612M 42+6	GROUND	33J34-2
33J31-12abc	41612M 42+6	DIGITAL ATTEN. CONTROL LSB	33J25-14a
33J31-13abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 2	33J25-15a
33J31-14abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 3	33J25-16a
33J31-15abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 4	33J25-17a
33J31-16abc	41612M 42+6	DIGITAL ATTEN. CONTROL MSB	33J25-18a
33J31-17abc	41612m 42+6	LOW PASS FILTER CONTROL IN	33J25-14c
33J31-18abc	41612M 42+6	CALIBRATION SWITCH CONTR. IN	33J25-15c
33J31-19abc	41612M 42+6	PHASE ADJUST SOURCE CONTROL	33J25-16c
33J31-20abc	41612M 42+6	NORMAL/TEST IF SELECT HIGH	33J25-17c
33J31-21abc	41612M 42+6	NORMAL/TEST IF SELECT LOW	33J25-18c
33J31-22abc	41612M 42+6	GROUND	33J34-2
33J31-23abc	41612M 42+6	-15 VDC BOARD POWER INPUT	33J34-3
33J56	BNC-F	IF TEST SIGNAL INPUT, 50 Ω	ON BOARD
33J57	BNC-F	I MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J58	BNC-F	Q MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J59	BNC-F	IF MONITOR OUTPUT, 50 Ω	ON BOARD

CHANNEL SEVEN BOARD CONNECTIONS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J20	MA-COM OSP	60 MHZ IF INPUT	33J7
33J32-2	41612M 42+6	60 MHZ REFERENCE INPUT	33J24-A7
33J32-5	41612M 42+6	I OUTPUT	33J10-A7
33J32-8	41612M 42+6	Q OUTPUT	33J11-A7
33J32-25	41612M 42+6	PHASE CONTROL VOLTAGE INPUT	33J25-28
33J32-28	41612M 42+6	OFFSET VIDEO OUTPUT	33J12-A7
33J32-31	41612M 42+6	IF SAMPLE OUTPUT	33J13-A7
33J32-10abc	41612M 42+6	+15 VDC BOARD POWER INPUT	33J34-1
33J32-11abc	41612M 42+6	GROUND	33J34-2
33J32-12abc	41612M 42+6	DIGITAL ATTEN. CONTROL LSB	33J25-14a
33J32-13abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 2	33J25-15a
33J32-14abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 3	33J25-16a
33J32-15abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 4	33J25-17a
33J32-16abc	41612M 42+6	DIGITAL ATTEN. CONTROL MSB	33J25-18a
33J32-17abc	41612m 42+6	LOW PASS FILTER CONTROL IN	33J25-14c
33J32-18abc	41612M 42+6	CALIBRATION SWITCH CONTR. IN	33J25-15c
33J32-19abc	41612M 42+6	PHASE ADJUST SOURCE CONTROL	33J25-16c
33J32-20abc	41612M 42+6	NORMAL/TEST IF SELECT HIGH	33J25-17c
33J32-21abc	41612M 42+6	NORMAL/TEST IF SELECT LOW	33J25-18c
33J32-22abc	41612M 42+6	GROUND	33J34-2
33J32-23abc	41612M 42+6	-15 VDC BOARD POWER INPUT	33J34-3
33J60	BNC-F	IF TEST SIGNAL INPUT, 50 Ω	ON BOARD
33J61	BNC-F	I MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J62	BNC-F	Q MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J63	BNC-F	IF MONITOR OUTPUT, 50 Ω	ON BOARD

CHANNEL EIGHT BOARD CONNECTIONS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J21	MA-COM OSP	60 MHZ IF INPUT	33J8
33J33-2	41612M 42+6	60 MHZ REFERENCE INPUT	33J24-A8
33J33-5	41612M 42+6	I OUTPUT	33J10-A8
33J33-8	41612M 42+6	Q OUTPUT	33J11-A8
33J33-25	41612M 42+6	PHASE CONTROL VOLTAGE INPUT	33J25-31
33J33-28	41612M 42+6	OFFSET VIDEO OUTPUT	33J12-A8
33J33-31	41612M 42+6	IF SAMPLE OUTPUT	33J13-A8
33J33-10abc	41612M 42+6	+15 VDC BOARD POWER INPUT	33J34-1
33J33-11abc	41612M 42+6	GROUND	33J34-2
33J33-12abc	41612M 42+6	DIGITAL ATTEN. CONTROL LSB	33J25-14a
33J33-13abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 2	33J25-15a
33J33-14abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 3	33J25-16a
33J33-15abc	41612M 42+6	DIGITAL ATTEN. CONTROL BIT 4	33J25-17a
33J33-16abc	41612M 42+6	DIGITAL ATTEN. CONTROL MSB	33J25-18a
33J33-17abc	41612m 42+6	LOW PASS FILTER CONTROL IN	33J25-14c
33J33-18abc	41612M 42+6	CALIBRATION SWITCH CONTR. IN	33J25-15c
33J33-19abc	41612M 42+6	PHASE ADJUST SOURCE CONTROL	33J25-16c
33J33-20abc	41612M 42+6	NORMAL/TEST IF SELECT HIGH	33J25-17c
33J33-21abc	41612M 42+6	NORMAL/TEST IF SELECT LOW	33J25-18c
33J33-22abc	41612M 42+6	GROUND	33J34-2
33J33-23abc	41612M 42+6	-15 VDC BOARD POWER INPUT	33J34-3
33J64	BNC-F	IF TEST SIGNAL INPUT, 50 Ω	ON BOARD
33J65	BNC-F	I MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J66	BNC-F	Q MONITOR OUTPUT, HIGH IMP.	ON BOARD
33J67	BNC-F	IF MONITOR OUTPUT, 50 Ω	ON BOARD

CONTROL BOARD CONNECTIONS

CONNECTOR DESIGNATION	TYPE	FUNCTION	DESTINATION CONNECTOR
33J22	MA-COM OSP	IF REFERENCE INPUT	33J9
33J23-1	DB-25 MALE	COMPUTER PARALLEL BIT 0	COMPUTER
33J23-2	DB-25 MALE	COMPUTER PARALLEL BIT 2	COMPUTER
33J23-3	DB-25 MALE	COMPUTER PARALLEL BIT 4	COMPUTER
33J23-4	DB-25 MALE	COMPUTER PARALLEL BIT 6	COMPUTER
33J23-5	DB-25 MALE	COMPUTER PARALLEL BIT 8	COMPUTER
33J23-6	DB-25 MALE	COMPUTER PARALLEL BIT 10	COMPUTER
33J23-7	DB-25 MALE	COMPUTER PARALLEL BIT 12	COMPUTER
33J23-8	DB-25 MALE	COMPUTER PARALLEL BIT 14	COMPUTER
33J23-9	DB-25 MALE	GROUND	COMPUTER
33J23-10	DB-25 MALE	GROUND	COMPUTER
33J23-11	DB-25 MALE	GROUND	COMPUTER
33J23-12	DB-25 MALE	GROUND	COMPUTER
33J23-13	DB-25 MALE	GROUND	COMPUTER
33J23-14	DB-25 MALE	COMPUTER PARALLEL BIT 1	COMPUTER
33J23-15	DB-25 MALE	COMPUTER PARALLEL BIT 3	COMPUTER
33J23-16	DB-25 MALE	COMPUTER PARALLEL BIT 5	COMPUTER
33J23-17	DB-25 MALE	COMPUTER PARALLEL BIT 7	COMPUTER
33J23-18	DB-25 MALE	COMPUTER PARALLEL BIT 9	COMPUTER
33J23-19	DB-25 MALE	COMPUTER PARALLEL BIT 11	COMPUTER
33J23-20	DB-25 MALE	COMPUTER PARALLEL BIT 13	COMPUTER
33J23-21	DB-25 MALE	COMPUTER PARALLEL BIT 15	COMPUTER
33J23-22	DB-25 MALE	GROUND	COMPUTER
33J23-23	DB-25 MALE	GROUND	COMPUTER
33J23-24	DB-25 MALE	GROUND	COMPUTER
33J23-25	DB-25 MALE	+5 VDC FOR MANUAL CONTROL	COMPUTER
33J24-A1	8W8 D-SHELL	CHANNEL 1 IF REFERENCE	33J26-2
33J24-A2	8W8 D-SHELL	CHANNEL 2 IF REFERENCE	33J27-2
33J24-A3	8W8 D-SHELL	CHANNEL 3 IF REFERENCE	33J28-2
33J24-A4	8W8 D-SHELL	CHANNEL 4 IF REFERENCE	33J29-2
33J24-A5	8W8 D-SHELL	CHANNEL 5 IF REFERENCE	33J30-2
33J24-A6	8W8 D-SHELL	CHANNEL 6 IF REFERENCE	33J31-2
33J24-A7	8W8 D-SHELL	CHANNEL 7 IF REFERENCE	33J32-2
33J24-A8	8W8 D-SHELL	CHANNEL 8 IF REFERENCE	33J33-2
33J25-2	41612M 24+8	CHANNEL 1 PHASE ADJUST	33J26-25
33J25-5	41612M 24+8	CHANNEL 2 PHASE ADJUST	33J27-25
33J25-8	41612M 24+8	CHANNEL 3 PHASE ADJUST	33J28-25
33J25-11	41612M 24+8	CHANNEL 4 PHASE ADJUST	33J29-25
33J25-22	41612M 24+8	CHANNEL 5 PHASE ADJUST	33J30-25
33J25-25	41612M 24+8	CHANNEL 6 PHASE ADJUST	33J31-25
33J25-28	41612M 24+8	CHANNEL 7 PHASE ADJUST	33J32-25
33J25-31	41612M 24+8	CHANNEL 8 PHASE ADJUST	33J33-25

33J25-13abc	41612M	24+8	+15 VDC BOARD POWER INPUT	33J34-1
33J25-14a	41612M	24+8	DIGITAL ATTEN. CONTROL LSB	33J26-12abc to 33J33-12abc
33J25-15a	41612M	24+8	DIGITAL ATT. CONTROL BIT 2	33J26-13abc to 33J33-13abc
33J25-16a	41612M	24+8	DIGITAL ATT. CONTROL BIT 3	33J26-14abc to 33J33-14abc
33J25-17a	41612M	24+8	DIGITAL ATT. CONTROL BIT 4	33J26-15abc to 33J33-15abc
33J25-18a	41612M	24+8	DIGITAL ATTEN. CONTROL MSB	33J26-16abc to 33J33-16abc
33J25-14c	41612M	24+8	LOW PASS FILTER CONTROL	33J26-17abc to 33J33-17abc
33J25-15c	41612M	24+8	CALIBRATION SWITCH CONTROL	33J26-18abc to 33J33-18abc
33J25-16c	41612M	24+8	PHASE ADJUST SQURCE CONTROL	33J26-19abc to 33J33-19abc
33J25-17c	41612M	24+8	NORMAL/TEST IF SELECT HIGH	33J26-20abc to 33J33-20abc
33J25-18c	41612M	24+8	NORMAL/TEST IF SELECT LOW	33J26-21abc to 33J33-21abc
33J25-19abc	41612M	24+8	GROUND	33J34-2
33J25-20abc	41612M	24+8	-15 VDC BOARD POWER INPUT	33J34-3

8.0 FIRST PROTOTYPE TEST

A preliminary design document was written. It covered the complete design of the SLC IF receiver in a block diagram format. From this the general design emerged and the detailed design was done. The receiver from the phase detector section to the outputs was designed first. A first prototype board with only this section on it was designed and built.

The first prototype board differs from the final prototype. The final prototype is the entire channel receiver board and has been designed and laid out as close to the final layout as possible. As of the writing of this section the first prototype has been thoroughly tested and the final prototype is about to be populated and tested.

The testing of the first prototype revealed several design flaws. These flaws were corrected and further testing was done. There were two major design changes made. The first was the choice of the IF gain block. Originally the Plessey SL560C IF amplifier was chosen as the general gain block for the IF section of the receiver. Its advantages were a variable gain, good noise figure and low cost. After testing it was decided not to use the SL560C for two reasons. The gain in a 50 ohm system was limited to +18 dB, not the +32 dB stated in the manual. The VSWR is also a relatively high 3:1 in a 50 ohm system since it has not been optimized for 50 ohms. The SL560C is better suited to a 75 ohm system.

The second major design change was in the offset video circuit. Originally an active high pass filter was used with an AD846. This produced a gain and increased the noise when more attenuation is actually needed. This high pass filter was changed to a simple RC high pass filter. It may be refined further after testing of the final prototype. Several other minor design changes were made, such as changing values of resistors or capacitors. It was found that the maximum output of the phase detectors was not as great as the Mini-Circuits handbook indicates. The maximum output is attainable only under ideal conditions when the optimum IF and reference signal levels are applied.

The HP4195A Network/Spectrum Analyzer was used for the bulk of the first prototype board testing. It was an invaluable measurement tool and saved much testing time. Some of the measurements made on the circuit could not have been done without the 4195A. The 4195A will be the main measurement tool for the final board testing and calibration. It has the capability of making hard copy plots via the HPIB interface bus and an external plotter. Copies of three of the many plots made are included in the following pages.

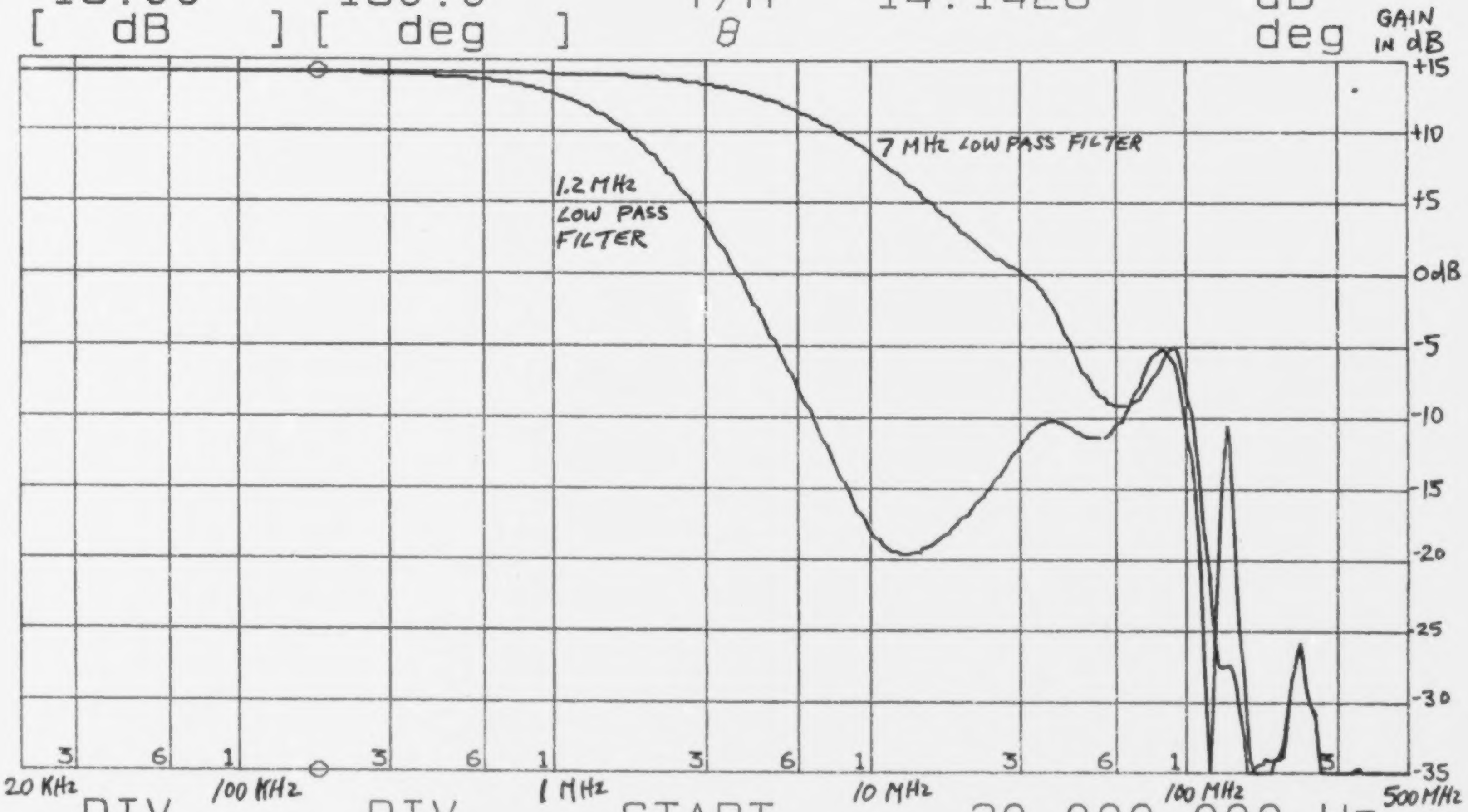
Plot A shows the two low pass filter responses. The -3 dB cutoff frequencies are at about 1.2 MHz and just over 7 MHz. There is a peak in the 1.2 MHz filter response at about 120 MHz. This can be reduced by optimizing the values of several capacitors on the final prototype. The rise to a peak just below 100 MHz is due to the board layout and parasitic reactances in the circuit.

Plot B is the offset video output frequency response, using the simple RC high pass filter and the 7 MHz low pass filter. The -3 dB bandwidth is from 532 kHz to 7.6 MHz. The cutoff frequencies can be changed by varying the values of the frequency determining capacitors in the low pass and high pass filters. The exact values will be determined during the final prototype board testing.

Plot C shows the noise output for the two low pass filters with no input, and without the phase detector section. The maximum noise level is -70 dBm, although up to 10 MHz it is below -75 dBm. This is a maximum peak-to-peak noise voltage of 200 microvolts.

The results of the first prototype test are in close agreement with the main specifications shown in section 2.0, except for the IF specifications. The final prototype has the full IF section on it. The exact passive component values can only be selected following testing of the final prototype board.

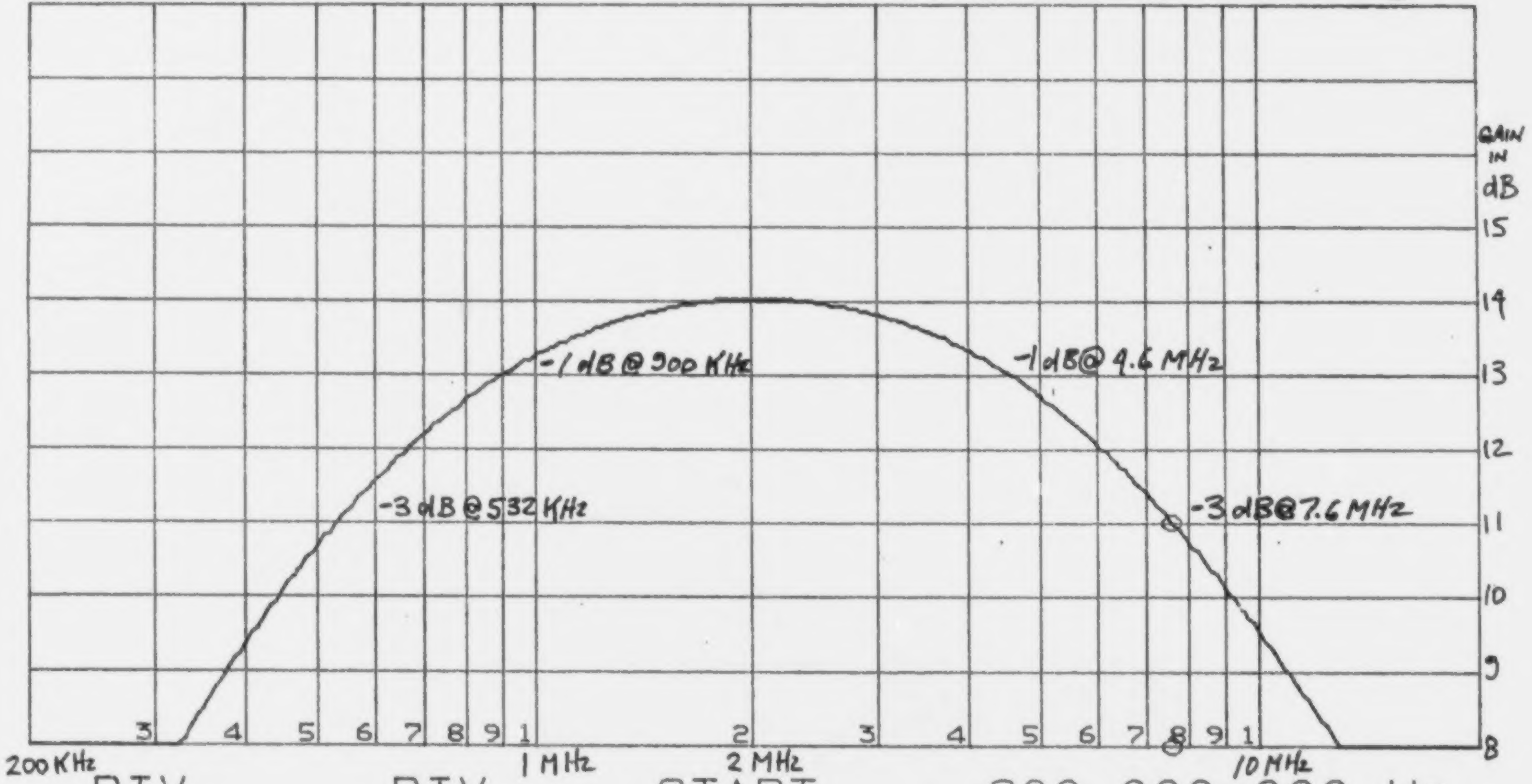
```
NETWORK    Cor
A: REF     B: REF       o MKR       176 435.957 Hz
  15.00      180.0        T/R    14.1428        dB
[  dB  ][  deg  ]         θ                     deg
```



```
 DIV           DIV          START         20 000.000 Hz
 5.000         36.00         STOP 500 000 000.000 Hz
RBW:  10 KHz  ST: 1.41  sec  RANGE: R=   0, T=   0dBm
REF=-6.00000E+01
```

PLOT A~ LOW PASS FILTER RESPONSES

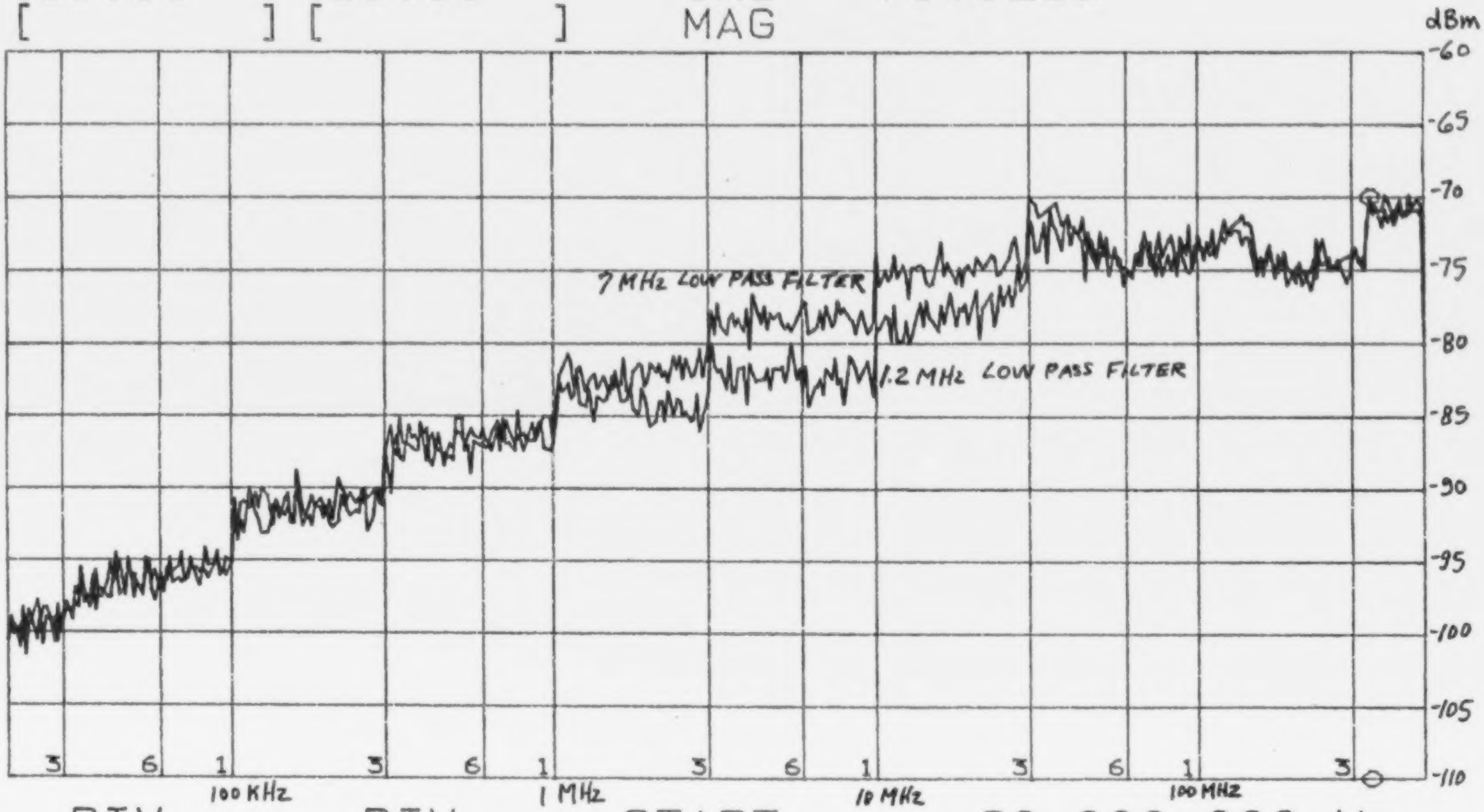
```
NETWORK      Cor
A: REF       B: REF          ○ MKR     7 603 787.926 Hz
 18.00        180.0            T/R     11.0157       dB
[  dB    ] [  deg    ]           8                   deg
```



```
 DIV          DIV          START       200 000.000 Hz
1.000        36.00          STOP    20 000 000.000 Hz
RBW:  10 KHz  ST: 1.41  sec  RANGE: R=  0, T=  0dBm
```

PLOT B~ OFFSET VIDEO OUTPUT RESPONSE

```
SPECTRUM      Math
A: REF      B: REF       o MKR 342 016 654.084 Hz
-60.00      -10.00         GAI   -70.0288
[          ] [          ]  MAG
```



```
  DIV          DIV        START          20 000.000 Hz
 5.000        10.00        STOP 500 000 000.000 Hz
RBW:  100 Hz  ST: 14.1 sec  RANGE: R=-10, T=-10dBm
REF=-6.00000E+01
```

PLOT C-NOISE OUTPUT

APPENDIX A

DATA FOR SUGGESTED DEVICES

COMPONENT DATA SHEETS INCLUDED

COMPONENT	DESCRIPTION	# USED	SOURCE OF DATA
MAN-1HLN	50 Ω LOW NOISE IF AMPLIFIER	41	92/93 RF/IF DESIGNER'S HANDBOOK, page 3-16
PSW-1211	PIN DIODE SPDT SWITCH	8	92/93 RF/IF DESIGNER'S HANDBOOK, page 13-10
TOSW-230	PIN DIODE SPDT SWITCH WITH INTERNAL TTL DRIVERS	9	92/93 RF/IF DESIGNER'S HANDBOOK, page 13-6
TSC-2-1	2-WAY, 0 DEGREE SPLITTER	8	92/93 RF/IF DESIGNER'S HANDBOOK, page 2-11
PSCQ-2-70	2-WAY, 90 DEGREE SPLITTER	8	92/93 RF/IF DESIGNER'S HANDBOOK, page 2-14
MPD-1	PHASE DETECTOR, + 7 dBm RF	16	92/93 RF/IF DESIGNER'S HANDBOOK, page 12-6
TDC-10-1	10 DB DIRECTIONAL COUPLER	1	92/93 RF/IF DESIGNER'S HANDBOOK, page 7-6
PSC-8-1	8-WAY, 0 DEGREE SPLITTER	1	92/93 RF/IF DESIGNER'S HANDBOOK, page 2-24
DA0857/B4	5 SECTION DIGITAL ATTENUATOR	8	DAICO 1992 PRODUCTS CATALOGUE, page 154
NE5204	HIGH FREQUENCY AMPLIFIER	16	SIGNETICS LINEAR DATA MANUAL, VOL. 1 1988 pg 4-3
PP-902	PHASE SHIFTER	8	SYNERGY 1992-93 CATALOGUE page 78
DCP-2B2	3-WAY, 0 DEGREE POWER DIVIDER	8	SYNERGY 1992-93 CATALOGUE page 84
VA-424A	MANUAL VARIABLE ATTENUATOR	8	LORCH ELECTRONICS RF AND IF SIGNAL PROCESSING COMPONENTS, CAT. #911, pg 16
AD842KN	WIDEBAND HIGH CURRENT OP-AMP	24	ANALOG DEVICES LINEAR PRODUCTS DATABOOK, 1990/91 page 2-267
AD846AN	HIGH SPEED PRECISION OP-AMP	32	ANALOG DEVICES LINEAR PRODUCTS DATABOOK, 1990/91 page 2-307
AD395JD	QUAD 12 BIT D/A CONVERTERS	2	ANALOG DEVICES DATA CONVERSION PRODUCTS DATABOOK 1989/90, pg 2-27
AD2701JD	-10.000 VDC REFERENCE	1	ANALOG DEVICES DATA CONVERSION PRODUCTS DATABOOK 1989/90, pg 8-67

COMPONENT	DESCRIPTION	# USED	SOURCE OF DATA
7812CTH	+12 VDC VOLTAGE REGULATOR	9	NATIONAL SEMICONDUCTOR LINEAR DATABOOK 1, 1987 page 1-251
7912CTH	-12 VDC VOLTAGE REGULATOR	8	NATIONAL SEMICONDUCTOR LINEAR DATABOOK 1, 1987 page 1-259
LM340LAH-5	+5 VDC VOLTAGE REGULATOR	8	NATIONAL SEMICONDUCTOR LINEAR DATABOOK 1, 1987 page 1-131
LM299AH	PRECISION REFERENCE	8	NATIONAL SEMICONDUCTOR LINEAR DATABOOK 2, 1987 page 7-76
KM6-II	UNIVERSAL SUBRACK, 6U HEIGHT	1	BICC-VERO 1992/3 ELECTRONICS HANDBOOK, page 3.07
DIN41612M	TYPE M DIN 41612 CONNECTORS	9	HARTING PRINTED-BOARD CATALOGUE # 03 5, page 40

broadband, linear

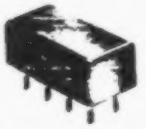
Low-Noise Amplifiers

up to 40mW (+16dBm) output
0.1 to 1000 MHz

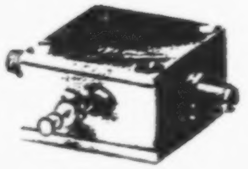
case style selection

outline drawings see Table of Contents

AMP



MAN



ZFL

	MODEL NO.	FREQUENCY MHz	GAIN, dB			MAX. POWER, dBm		DYNAMIC RANGE		VSWR		DC POWER		PRICE $	DISTRIBUTOR	
				Flatness Max.												
		f_L f_U	Min.	m	Total Range	Output (1 dB Comp.)	Input (no damage)	NF dB Typ.	IP3 dBm Typ.	In	Out	Volt. V.	Current mA	Qty. (1-9)	FACTORY	LOCAL
AMP	AMP-11-2	5-1000	14	±1.0	±1.0	−3.5	+13	3.0	+13	2:1	2:1	15	12	44.95	●	
case PP120	AMP-15	5-1000	13	±0.6	±1.2	+8.0	+13	2.8	+22	2:1	2:1	15	29	40.95	●	
	AMP-75	5-500	19	±0.4	±1.0	+12.0	+13	2.4	+28	2:1	2:1	15	29	43.95	●	
	AMP-76	5-500	26	±0.7	±1.0	+13.5	+6	3.1	+28	2:1	2:1	15	68	78.95	●	
	AMP-77	5-500	15	±0.4	±1.0	+16.0	+13	3.3	+32	2:1	2:1	15	56	45.95	●	
MAN	MAN-1LN	0.5-500	28	±0.5	±1.0	+8	+15	2.8	+18	1.8:1	1.8:1	12	60	19.95	●	●
case A05	MAN-1HLN●	10-500	10	±0.5	±0.8	+15	+15	3.7	+30	1.8:1	1.8:1	12	70	19.95	●	●
ZFL	ZFL-500HLN	10-500	19	—	±0.4	+16	+15	3.8	+30	1.5:1	1.5:1	15	110	99.95	●	
-	ZFL-500LN	0.1-500	24	—	±0.3	+5	+5	2.9	+14	1.5:1	1.6:1	15	60	79.95	●	
case Y39	ZFL-1000LN	0.1-1000	20	—	±0.5	+3	+5	2.9	+14	1.5:1	2:1	15	60	89.95	●	

L_W = Low Range (f_L to $f_{u/2}$)   m = mid Range (2 f_L to $f_{u/2}$)   U = Upper Range ($f_{u/2}$ to f_u)

features

- ideal for printed-circuit designs (MAN & AMP series)
- smooth response over entire band, no external resonances
- low impedance, less susceptible to EMI
- easy to use, 50 ohm input/output
- all models are cascadable

NOTES:

** VSWR 1.6 maximum from 01. to 0.2 MHz.
Also available with BNC connectors. $5.00 additional

● case A06

1. For quality control procedures, environmental specifications, see Table of Contents.
2. Absolute Maximum Ratings, see Environmental Specifications page 3-13.
3. Prices and specifications subject to change without notice.
4. Maximum Operating Temperature for AMP series: −54°C-+85°C.
5. Maximum DC Voltage: 17V for AMP series, 12.5V for MAN series.

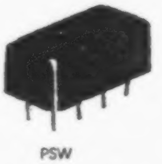
PIN CONFIGURATION

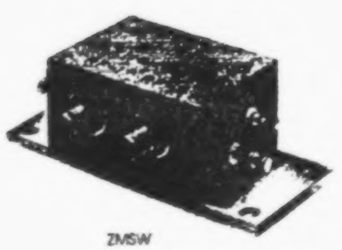
SERIES	MAN	AMP
RF IN	1	2
RF OUT	8	4
DC	5	1
CASE GND	2,3,4,6	3
NOT USED	7	—

Switches

SPST/SPDT pin diode
10 to 2500 MHz

case style selection
outline drawings see Table of Contents


PSW


ZMSW

	MODEL NO.	TYPE	FREQUENCY MHz f_L-f_U	INSERTION LOSS dB low-band lw Typ.	INSERTION LOSS dB low-band lw Max.	INSERTION LOSS dB upper band U Typ.	INSERTION LOSS dB upper band U Max.	IN-OUT ISOLATION dB L Typ.	IN-OUT ISOLATION dB L Min.	IN-OUT ISOLATION dB M Typ.	IN-OUT ISOLATION dB M Min.	IN-OUT ISOLATION dB U Typ.	IN-OUT ISOLATION dB U Min.	PRICE $ Qty. (1-9)	DISTRIBUTOR FACTORY	DISTRIBUTOR LOCAL
PSW case A06	PSW-1111	SPST	10-2500	1.1	1.7	1.7	2.7	50	40	35	30	28	22	32.95	●	●
	PSW-1211	SPDT	10-2500	1.1	1.7	1.7	2.7	50	40	35	30	28	22	32.95	●	●
ZMSW case JJ77	ZMSW-1111	SPST	10-2500	1.1	1.7	1.7	2.7	50	45	35	30	28	22	69.95	●	
	ZMSW-1211	SPDT	10-2500	1.1	1.7	1.7	2.7	50	45	35	30	28	22	69.95	●	

L=low range (f_L to 10 f_L) M=mid range (10f_L to $f_U/2$) U=upper range ($f_U/2$ to f_U)
lw=low band (f_L to $f_U/2$)

NOTES:
1. Refer to Table of Contents for quality control procedures, environmental specifications, absolute maximum ratings, and hi-rel testing.
2. For PSW and ZMSW models
   a) VSWR 1.6 max. ("on" state)
   b) Switching time 4μ sec. max., 2μ sec. rise time.
   c) Maximum RF input +20 dBm
   d) Control voltage +5V (5mA max.) on condition
      0V off condition
3. 1 dB compression for all pin diode switches from 10 to 100 MHz increase from 6 to 19 dBm. Above 100 MHz, 19 dBm min.
4. Prices and specifications subject to change without notice.

NSN GUIDE

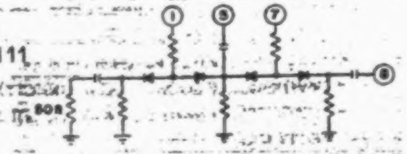
MCL NO.	NSN
PSW-1211	5985-01-328-8006

pin and coaxial connections
see case style outline drawings

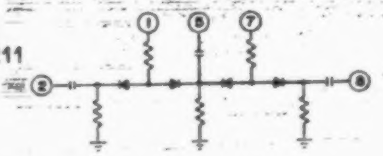
Series	PSW		ZMSW	
Models	1111	1211	1111	1211
RF COMMON	5	5	com	com
RF-1 port	8	2	—	RF-1
RF-2 port	—	8	RF-2	RF-2
CONTROL RF-1	7	1	—	1
CONTROL RF-2	—	7	2	2
CONTROL 50 ohm TERMINATION	1	—	1 —	— —
GND	2,4	4	—	—
CASE GND	3,6	3,6	—	—

schematic

Model PSW-1111



Model PSW-1211

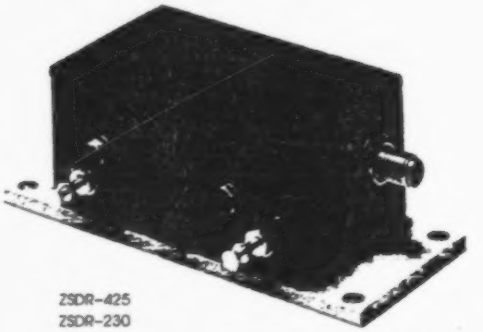


Switches, with TTL Drivers

SPDT/SP4T
pin diode
10 to 3000 MHz

case style selection
outline drawings see Table of Contents

TOSW

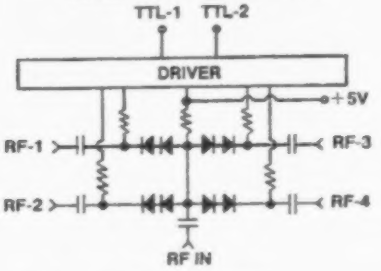

ZSDR-425
ZSDR-230

MODEL NO.		TYPE	FREQUENCY MHz	INSERTION LOSS dB				IN-OUT ISOLATION dB						PRICE $	DISTRIBUTOR	
				low-band lw		upper band U		L		M		U				
			f_L-f_U	Typ.	Max.	Typ.	Max.	Typ.	Min.	Typ.	Min.	Typ.	Min.	Qty. (1-9)	FACTORY	LOCAL
TOSW	TOSW-230	SPDT	10-3000	1.3	1.9	1.8	2.7	60	40	40	28	35	22	49.95	●	●
case QQ96	TOSW-425	SP4T	10-2500	1.1	1.7	1.5	2.5	60	40	40	30	35	22	69.95	●	●
ZSDR																
case CCC-127	ZSDR-230	SPDT	10-3000	1.3	1.9	1.8	2.7	60	40	40	28	35	22	89.95	●	
case GGG-126	ZSDR-425	SP4T	10-2500	1.1	1.7	1.5	2.5	60	40	40	30	35	22	109.95	●	

L=low range (f_L to 10 f_L) M=mid range (10f_L to $f_U/2$) U=upper range ($f_U/2$ to f_U)
lw=low band (f_L to $f_U/2$)

ADDITIONAL SPECIFICATIONS
VSWR ("on" state): typ. 1.3, 1.6 max.
Switching time (μ sec): all switches, typ. 2.0, 4.0 max.
Max. RF input for all switches: 20 dBm for low range, 28 dBm for mid range, & 30 dBm for upper range.
Supply voltage for all switches, +5V (10 mA max.)
1 dB compression point for all switches: from 10-100 MHz increase from 6 to 19 dBm. Above 100 MHz, 19 dBm min.
TTL input high threshold 2 volts min.
TTL input low threshold 0.8 volts max.

MODEL TOSW-425 & ZSDR-425



TTL LOGIC FOR ZSDR-425 & TOSW-425

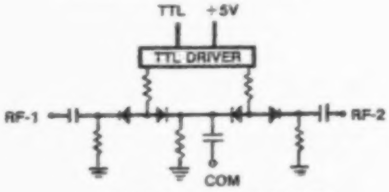
	TTL-1	TTL-2
RF-1	1	0
RF-2	1	1
RF-3	0	1
RF-4	0	0

pin connections
see case style outline drawings

Series	TOSW	
Models	425	230
RF IN	8	8
RF-1	4	5
RF-2	6	11
RF-3	10	—
RF-4	12	—
TTL-1	2	3*
TTL-2	3	—
+5 VDC	1	1
CASE GND	5,7,9,11	2,4,6,7, 9,10,12

*TTL: pin 3

MODEL TOSW-230 & ZSDR-230



TTl LOGIC FOR ZSDR-230 & TOSW-230

TTL 1:	RF-1/OFF	RF-2/ON
TTL 0:	RF-1/ON	RF-2/OFF

NOTES:
1. Refer to Table of Contents for quality control procedures, environmental specifications, absolute maximum ratings, and hi-rel testing
2. Prices and specifications subject to change without notice.

50 ohms and 75 ohms

Mini-Circuits

MSC-2

TSC-2

SCP-2

TO5SC-2

	MODEL NO.	FREQ. RANGE MHz	ISOLATION dB						INSERTION LOSS, dB Above 3dB						PHASE UNBALANCE Degrees			AMPLITUDE UNBALANCE dB			PRICE $	DISTRIBUTOR	
			L		M		U		L		M		U		L	M	U	L	M	U		FACTORY	LOCAL
		f_L–f_U	Typ.	Min.	Typ.	Min.	Typ.	Min.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Max.	Max.	Max.	Max.	Max.	Max.	Qty. (1–9)		
MSC-2 case A03	MSC-2-1	0.1–450	20	15	30	20	30	20	0.3	0.5	0.4	0.75	0.6	1.0	2.0	3.0	4.0	0.15	0.2	0.3	18.95	●	●
	MSC-2-1W	2–650	22	18	30	20	22	18	0.3	0.5	0.5	0.8	0.8	1.2	1.0	2.0	4.0	0.3	0.2	0.3	20.95	●	●
	MSC-2-5	5–1500	18	16	20	16	20	14	0.6	0.8	0.6	0.8	0.6	1.1	2.0	3.0	5.0	0.2	0.3	0.4	24.95	●	●
	MSC-2-11	5–2000	18	16	20	16	18	11	0.6	0.8	0.6	0.8	1.2	1.8	2.0	3.0	5.0	0.2	0.3	0.5	29.95	●	●
TSC-2 case B02	TSC-2-1	1–400	30	25	30	25	30	20	0.25	0.5	0.4	0.75	0.8	1.0	2.0	3.0	4.0	0.15	0.2	0.6	15.95	●	●
☐oSCP-2 case YY101	SCP-2-1	0.1–400	25	15	30	20	25	20	0.3	1.2	0.2	0.6	0.4	1.1	2.0	2.0	3.0	0.15	0.2	0.3	10.45	●	●
	SCP-2-1A	1–550	25	20	25	20	25	20	0.3	0.6	0.3	0.6	0.7	1.3	2.0	2.0	3.0	0.15	0.2	0.4	10.45	●	●
TO5SC-2 case LL163	TO5SC-2-1	1–500	30	20	28	20	26	20	0.2	0.5	0.3	0.7	0.7	1.5	2.0	1.0	2.5	0.25	0.25	0.4	24.95	●	●

L = low range (f_L to 10 f_L) M = mid range (10 f_L to $f_U/2$) U = upper range ($f_U/2$ to f_U)

pin connections

see case style outline drawing

Series	Sum Port	Port 1	Port 2	Case Ground
LPS	1	4	5	2,3,6,7,8
▼LRPS	6	4	3	—
PSC-2	1	5	6	2,3,4,7,8
MSC-2	1	5	6	2,3,4,7,8
SCP-2-1	1	5	6	2,3,4,7,8
TSC-2	1	2	4	3
TO5SC-2	2	1	3	4,5

MIL-P-23971/15, NSN GUIDE

MCL NO.	NSN	MIL-P-23971/15*
MSC-2-1	6625-01-124-8595	02
PSC-2-1	6625-00-548-0739	01
PSC-2-1W	5985-01-190-7701	
PSC-2-2	6625-01-143-2571	
PSC-2-4	6625-01-230-0492	
TSC-2-1	5895-01-332-8100	

* units are not QPL listed

In Stock...Immediate Delivery

now available computer-automated performance data

Power Splitter/Combiners

2 WAY–90°

0.42 MHz to 4.2 GHz

case style selection

outline drawings see Table of Contents

SYPQ

PSCQ-2

SCPQ

LRPQ

	MODEL NO.	FREQ. RANGE MHz	ISOLATION dB		INSERTION LOSS, dB Avg. of Coupled Outputs less 3 dB		PHASE UNBALANCE	AMPLITUDE UNBALANCE	PRICE $	DISTRIBUTOR	
			Typ.	Min.	Typ.	Max.	Degrees Max.	dB Max.	Qty. (1–9)	FACTORY	LOCAL
PSCQ-2 case A01	PSCQ-2-0.455	0.42–0.51	30	25	0.1	0.5	3.0	1.2	25.95		
	PSCQ-2-1.25	1.13–1.38	29	25	0.4	0.7	3.0	1.2	14.95	●	●
	PSCQ-2-1.5	1.4–1.7	29	25	0.4	0.7	3.0	1.2	14.95	●	●
	PSCQ-2-3.4	3.0–3.8	30	25	0.4	0.7	3.8	1.2	19.95	●	●
	PSCQ-2-4.0	3.5–4.5	36	25	0.4	0.7	3.0	1.5	14.95	●	●
	PSCQ-2-6.4	5.8–7.0	30	25	0.4	0.7	3.0	1.2	14.95	●	●
	PSCQ-2-7.5	7.0–8.0	35	25	0.4	0.7	3.0	1.2	14.95	●	●
	PSCQ-2-10.5	9.0–11.0	25	20	0.4	0.7	3.0	1.2	14.95	●	●
	PSCQ-2-13	12–14	29	25	0.4	0.7	3.0	1.2	14.95	●	●
	PSCQ-2-14	12–16	30	25	0.3	0.6	3.0	1.8	19.95	●	●
	PSCQ-2-17.5	16–19	28	25	0.6	0.7	3.0	1.6	14.95	●	●
	PSCQ-2-21.4	20–23	30	25	0.4	0.7	3.0	1.2	14.95	●	●
	PSCQ-2-26	14–30	25	20	0.4	0.7	3.0	1.5	23.95	●	●
	PSCQ-2-40	23–40	21	18	0.3	0.7	3.0	1.5	19.95	●	●
	PSCQ-2-50	25–50	30	20	0.3	0.7	3.0	1.5	23.95	●	●
	PSCQ-2-70	40–70	30	20	0.3	0.7	3.0	1.5	23.95	●	●
	PSCQ-2-70N	66–74	22	19	0.2	0.5	0.8	0.25	23.95	●	●
	PSCQ-2-90	55–90	30	20	0.3	0.7	3.0	1.2	23.95	●	●
	PSCQ-2-120	80–120	25	18	0.3	0.7	3.0	1.5	23.95	●	●
	PSCQ-2-160	100–160	24	19	0.3	0.7	3.0	1.5	23.95	●	●
	PSCQ-2-180	120–180	23	15	0.3	0.7	4.0	1.2	23.95	●	●
	PSCQ-2-250	150–250	30	22	0.4	0.8	4.0	1.5	23.95	●	●
	PSCQ-2-300	220–300	27	20	0.3	0.7	3.0	1.3	23.95	●	●
	PSCQ-2-400	250–400	23	16	0.5	0.9	4.0	1.5	23.95	●	●
	PSCQ-2-450	350–450	23	16	0.5	0.9	5.0	1.5	23.95	●	●
	PSCQ-2-550	450–550	19	15	0.4	0.7	5.0	1.5	23.95	●	●
case A05	PSCQ-2-1000	800–1000	27	20	0.28	0.6	3.0	1.3	25.95	●	●
noSCPQ case YY101	SCPQ-21.4	20–23	32	25	0.15	0.5	2.5	1.0	13.95	●	●
	SCPQ-90	55–90	26	20	0.2	0.7	3.0	1.2	13.95	●	●
	●SCPQ-180	120–180	20	16	0.3	0.7	3.0	1.2	13.95	●	●
	●SCPQ-400	250–400	20	16	0.3	0.7	3.0	1.2	14.95	●	●
•noLRPQ case QQQ130	LRPQ-70	65–75	30	20	0.1	0.5	3.0	1.0	9.95	●	●
	LRPQ-700	500–700	23	18	0.2	0.6	3.0	1.5	9.95	●	●
	LRPQ-980	820–980	28	20	0.15	0.5	4.0	1.0	11.95	●	●
uoSYPQ case AH202	SYPQ-21.4	20–23	33	25	0.1	0.4	3.0	1.1	13.95	●	●
	SYPQ-70	65–75	31	24	0.1	0.4	3.0	1.1	13.95	●	●

Models available at frequencies other than shown in chart above. Please consult factory highest figure of merit

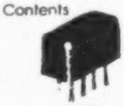
Phase Detectors

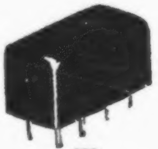
1000mV DC output, +7dBm RF

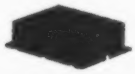
case style selection

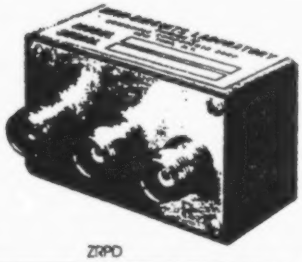
outline drawings see Table of Contents

LPD


MPD


RPD


SYPD


ZRPD

	MODEL NO.	FREQUENCY MHz RF1 RF2	FREQUENCY MHz I	POWER IN RF1 RF2 (dBm)	SCALE FACTOR mV/degree	IMPEDANCE (ohms) OUTPUT LOAD I	ISOLATION (dB) RF1 - RF2 Min.	OUTPUT POLARITY (RF1/RF2 in-phase)	DC OUTPUT (mV) Max. Typ.	DC OUTPUT (mV) Max. Min.	DC OUTPUT (mV) OFFSET Typ.	DC OUTPUT (mV) OFFSET Max.	FIGURE-OF-MERIT M Typ.	PRICE $ Qty. (1-9)	DISTRIBUTOR FACTORY	DISTRIBUTOR LOCAL
LPD case BB48	LPD-1	1-100	DC-50	+7	8	500	40	neg	1000	750	0.2	1	143	26.45	●	●
MPD case A11	MPD-1	1-100	DC-50	+7	8	500	40	neg	1000	750	0.2	1	143	21.45	●	●
	MPD-2	10-200	DC-50	+7	8	500	40	neg	1000	750	0.3	1	143	24.95	●	●
	MPD-21	50-400	DC-50	+7	7	500	40*	neg	800	600	0.5	1	120	26.95	●	●
RPD case A01	RPD-1	1-100	DC-50	+7	8	500	40	neg	1000	750	0.2	1	143	18.45	●	●
	RPD-2	5-150	DC-50	+7	8	500	40	neg	1000	750	0.3	1	143	20.95	●	●
□ SYPD case TT1167	SYPD-1	1-100	DC-50	+7	8	500	40	neg	1000	750	0.2	1	143	14.95	●	●
	SYPD-2	10-200	DC-50	+7	8	500	40	neg	1000	750	0.3	1	143	18.95	●	●
ZRPD case M22	ZRPD-1	1-100	DC-50	+7	8	500	40	neg	1000	750	0.2	1	143	57.95	●	

RF1 = RF input RF2 = RF reference

NOTES:
□ NON-HERMETIC
* 30 dB, 200 to 400 MHz
1. Maximum RF input power, 50 mW, peak IF current, 20mA.
2. Refer to Table of Contents for quality control procedures, environmental specifications, absolute maximum ratings, and hi-rel testing
3. Prices and specifications subject to changewithout notice.

NSN GUIDE

MCL NO.	NSN
MPD-1	6625-01-294-7152
RPD-1	5895-01-250-8525

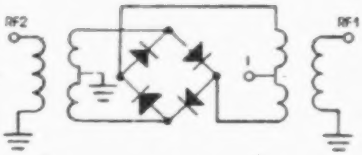
pin connections

see case style outline drawing

Series		RPD	MPD	LPD	SYPD
RF REF.	RF2	8	8	8	2
RF in:	RF1	1	1	5	1
DC out:	I	*3,4	*3,4	4	3
GND◆		2,5,6,7	2,5,6,7	1,2,3,6,7	4,5,6
CASE GND.		2	2	1,2,3,6,7	—

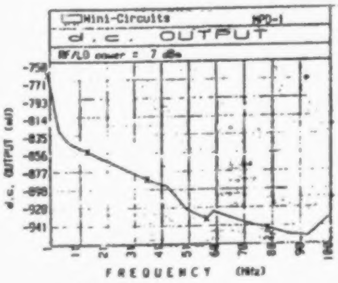
◆Ground externally. All measurements made with GND pin(s) grounded externally.
*pins must be externally connected together

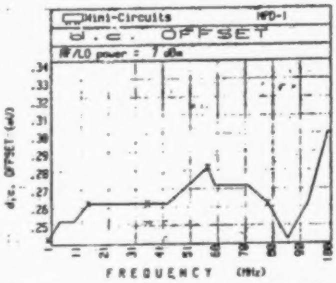
schematic

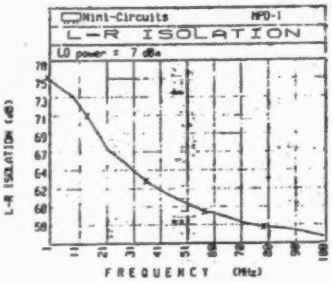


LPD-1, MPD-1, RPD-1, ZRDP-1, SYPD-1

1 to 100 MHz



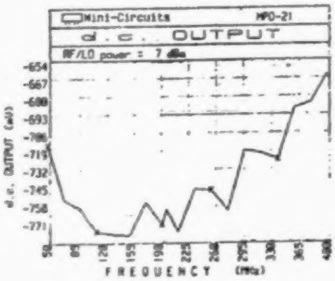


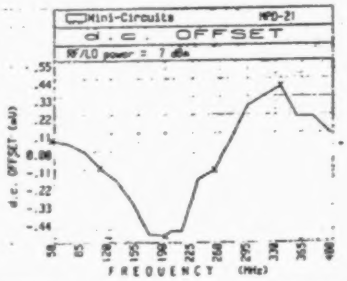


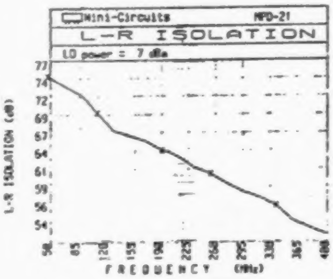
FREQUENCY	DC OUTPUT		DC OFFSET		L-R ISOLATION
	X̄	σ	X̄	σ	X̄
(MHz)	(mV)	(mV)	(mV)	(mV)	(dB)
1.000	-769.98	14.85	0.10	0.16	76.12
5.000	-830.34	8.90	0.11	0.18	75.09
8.071	-840.24	14.44	0.11	0.18	74.07
10.000	-843.71	14.61	0.10	0.18	73.19
15.143	-851.12	17.01	0.11	0.19	70.19
20.000	-859.20	18.91	0.11	0.19	68.10
22.214	-861.26	20.52	0.10	0.20	67.28
29.286	-872.02	22.55	0.11	0.21	65.14
36.357	-881.57	24.77	0.11	0.22	63.29
40.000	-886.86	25.39	0.12	0.23	62.38
43.429	-889.93	26.41	0.12	0.23	61.76
50.500	-917.82	25.99	0.14	0.25	60.51
57.571	-927.50	28.69	0.15	0.27	59.35
60.000	-917.14	33.08	0.15	0.26	59.18
64.643	-920.62	38.60	0.15	0.27	58.73
71.714	-925.22	45.18	0.17	0.31	57.82
78.786	-928.03	51.83	0.18	0.31	57.35
85.857	-932.34	57.31	0.17	0.31	57.15
92.929	-932.98	60.65	0.18	0.38	56.93
100.000	-909.17	74.27	0.23	0.43	56.36

MPD-21

50 to 400 MHz







FREQUENCY	DC OUTPUT		DC OFFSET		L-R ISOLATION
	X̄	σ	X̄	σ	X̄
(MHz)	(mV)	(mV)	(mV)	(mV)	(dB)
50.000	-709.82	3.59	0.08	0.04	70.65
70.588	-749.08	3.90	0.05	0.06	67.43
91.176	-754.30	4.74	-0.01	0.08	66.33
100.000	-761.44	5.14	-0.05	0.08	65.36
111.765	-768.79	5.90	-0.11	0.09	64.25
132.353	-768.89	7.05	-0.20	0.10	61.88
152.941	-767.63	8.30	-0.34	0.11	61.49
173.529	-742.21	9.53	-0.48	0.14	60.94
194.118	-755.32	11.20	-0.45	0.18	60.49
200.000	-744.32	11.29	-0.41	0.18	60.16
214.706	-758.79	12.19	-0.39	0.23	59.51
235.294	-727.66	13.02	-0.08	0.17	57.81
255.882	-725.26	15.07	-0.03	0.18	57.03
276.471	-736.71	17.30	0.14	0.15	55.98
297.059	-692.38	18.31	0.27	0.09	54.45
317.647	-691.52	20.64	0.31	0.11	53.62
338.235	-694.23	21.94	0.34	0.14	52.91
358.824	-656.91	21.62	0.19	0.10	52.02
379.412	-652.04	21.74	0.19	0.12	51.31
400.000	-632.47	20.37	0.11	0.09	50.99

very broadband

Directional Couplers

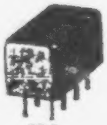
6 to 30 dB

5 KHz to 2000 MHz

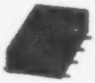
case style selection

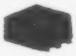
outline drawings see Table of Contents

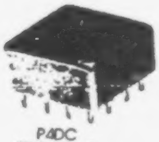
TDC


PDC

TODC


SCDC


LRDC


P4DC
PDC-20A-5

	MODEL NO.	FREQ. MHz f_L-f_U	COUPLING dB Nom	COUPLING dB Flatness	MAINLINE LOSS* dB L Typ.	L Max.	M Typ.	M Max.	U Typ.	U Max.	DIRECTIVITY dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	VSWR (:1) Typ.	POWER INPUT, W L Max.	MU Max.	PRICE $ Qty. (1-9)	DISTRIBUTOR FACTORY	LOCAL
TDC	TDC-6-1	10-400	6.3±0.4	±0.4	2.0	2.4	2.0	2.4	2.0	2.5	36	30	30	25	20	15	1.5	1	2	23.95	●	●
case 802	TDC-10-1	1-400	10.0±0.5	±0.5	1.2	1.5	1.0	1.3	1.2	1.5	35	25	30	20	20	15	1.5	1	2	17.95	●	●
	TDC-10-2	5-1000	11±0.5	±0.6	1.4	1.8	1.5	1.8	1.6	2.0	50	35	25	20	20	15	1.5	0.5	0.5	25.95	●	●
PDC	PDC-10-1	0.5-500	11.5±0.5	±0.6	0.85	1.3	0.65	1.0	0.85	1.3	32	25	32	25	22	15	1.2	1.5	3	13.45	●	●
◇◇	PDC-10-18D	1-400	11.5±0.5	±0.5	0.6	0.9	0.8	1.1	0.9	1.3	55	35	35	20	22	15	1.2	2.0	4	11.45	●	●
case A01 :	PDC-10-2	250-1000	10.5±0.5	±0.6	1.4	1.6	—	—	1.6	2.0	30	23	30	20	25	15	1.5	—	5	34.45	●	●
	PDC-10-5	1-2000	10.5±0.5	±1.0	1.2	1.9	1.3	1.9	2.0	2.5	38	25	30	18	22	18	1.3	0.5	0.5	40.95	●	●
	PDC-10-6	0.005-20	11±0.5	±0.5	0.4	1.2	0.4	0.8	0.4	1.0	40	30	40	30	35	25	1.3	1.5	3	23.95	●	●
	PDC10-21	1-1000	11±0.5	±0.5	1.2	1.7	1.2	1.7	1.6	2	40	30	25	20	25	20	1.3	1	2	32.95	●	●
	PDC-10-22	5-750	11±0.5	±0.5	1.1	1.6	1.2	1.7	1.6	1.9	35	30	25	20	25	20	1.25	1	2	23.95	●	●
	PDC-10-54	10-1500	10.5±0.5	±0.7	1.2	1.8	1.3	1.9	1.6	2.3	35	25	28	23	28	23	1.3	0.5	0.5	35.95	●	●
	PDC-15-6	0.01-35	15±0.5	±0.5	0.3	0.6	0.2	0.4	0.3	0.6	38	30	35	25	28	20	1.15	2	4	23.95	●	●
	PDC-15-21	1-500	14.7±0.5	±0.6	0.7	1.1	0.7	1.1	0.8	1.2	35	30	35	30	30	23	1.4	1	2	23.95	●	●
††	PDC-20-1	25-400	21±0.75	±0.5	0.2	0.25	0.3	0.35	0.35	0.5	25	20	35	25	25	20	1.25	3	5	23.95	●	●
◇◇	PDC-20-18D	0.5-200	19.2±0.5	±0.5	0.3	0.5	0.3	0.5	0.4	0.6	40	30	35	20	18	22	1.1	3	5	16.95	●	●
	PDC-20-1W	10-700	19.2±0.5	±0.5	0.25	0.5	0.4	0.7	0.7	1.1	34	30	27	23	23	20	1.4	1	2	23.95	●	●
	PDC-20-3	0.2-250	19.5±0.5	±0.5	0.35	0.6	0.25	0.5	0.35	0.6	36	30	33	25	25	20	1.2	1.5	4	15.95	●	●
◇◇	PDC-20-38D	0.2-250	19.5±0.5	±0.5	0.3	0.6	0.25	0.5	0.35	0.6	47	40	40	25	30	20	1.1	1.5	4	17.95	●	●
case ■145	PDC-20A-5	0.1-2000	20.0±0.5	±1.0	0.6	1.5	0.6	1.5	1.9	2.9	34	20	25	15	20	10	1.5	0.5	2	44.95	●	●
case A01	■ PDC-10-1-75	1-250	10.5±0.5	±0.75	1.1	1.5	1.1	1.5	1.1	1.5	30	20	30	20	30	20	2.0	2	4	14.95	●	●
	■ PDC-10-6-75	0.2-100	10.0±0.5	±0.2	1.2	1.6	0.9	1.2	0.9	1.3	50	30	40	25	37	25	1.5	1	2	23.95	●	●
	■ PDC-15-6-75	0.02-35	14.5±0.5	±0.5	0.3	0.7	0.3	0.7	0.3	0.7	35	20	35	20	35	20	1.3	1.5	4	25.95	●	●
	■ PDC-20-3-75	1-150	19.5±0.5	±0.75	0.35	0.8	0.35	0.8	0.35	0.8	25	20	25	20	25	20	2.0	2	4	14.95	●	●
	■ PDC-20-6-75	0.05-40	20.4±0.3	±0.25	0.1	0.25	0.1	0.2	0.1	0.3	45	35	35	20	25	18	1.2	1.5	3	23.95	●	●
TODC case QQ96	TODC-10-1	10-400	11.3±0.5	±0.5	1.2	1.5	1.0	1.3	1.2	1.5	35	25	30	20	25	20	1.5	0.5	1	17.95	●	●
□○SCDC	SCDC-11-2	500-1100	11.3±0.5	±0.6	—	—	1.1	1.8**	—	—	—	—	20	14**	—	—	1.4	2	2	11.95	●	●
case YY161	SCDC-25-2	500-1090	25.5±0.75	±0.8	—	—	0.5	1.0**	—	—	—	—	22	10**	—	—	1.4	2	2	13.95	●	●
□○LRDC case QQQ130	LRDC-20-2	300-1100	20.5±1.0	±1.3	—	—	0.25	0.6**	—	—	—	—	22	10**	—	—	1.2	2	2	15.95	●	●
▼P4DC case C07	P4DC-30A-2	5-1000	30.5±0.5	±1	0.7	1.2	0.7	1.2	0.8	1.5	30	15	32	20	20	10	1.15	1	2	34.95	●	●

L=low range (f_L to 10 f_L)   M=mid range (10 f_L to $f_U/2$)   U=upper range ($f_U/2$ to f_U)

pin and coaxial connection

see case style outline drawing

Series	In	Out	Cpl_{in}	◇◇ Cpl_{out}	Case Ground	Not Used
TODC	5	8	2	—	all others	11
PDC	1	4	3	6	2,5,7,8	6
TDC	1	2	4	—	3	—
ZEDC	1	2	3	—	—	—
ZMDC	3	2	1	—	—	—
ZDC	3	2	1	—	—	—
SCDC	1	2	5	—	4,7,8	3,6
ZFDC (except 20-4, -5)	1	2	3	—	—	—
ZFDC-20-4, -5	3	1	2	—	—	—
PDC-20A-5	9	5	12	—	1,2,3,4,6,7,8,10,11	—
▼P4DC-30A-2	8	12	—	—	—	—
LRDC-20-2	6	1	4	—	2,5	3

NOTES:

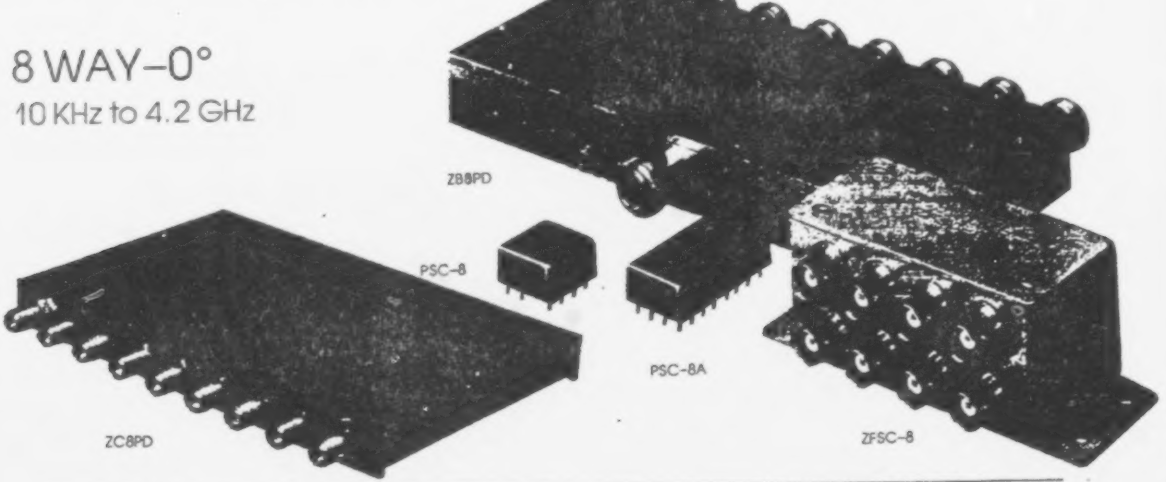
□ **NON-HERMETIC**
○ Available on tape and reel, please consult factory.
: $L = f_L - 2f_L$
* Includes theoretical power loss at coupled port.
■ Denotes 75 ohm models, available only with 75 ohm BNC
∴ bi directional, L = 30 to 100 MHz
◇◇ bi directional
†† Models PDC-20-1, ZDC-20-1, ZMDC-20-1: L=25-50 MHz, M=50-300 MHz, U=300-400 MHz
● Model ZFDC-20-5: above 1000 MHz, coupling flatness ±1.0dB Models PDC-10-21, ZFDC-10-21: Upper range coupling ±0.75dB
** Mainline loss and directivity are specified for total frequency range
▼ 4 coupled ports, 25 dB min. isolation between ports. Cpl #1, pin 2; Cpl #2, pin 1; Cpl #3, pin 13; Cpl #4, pin 14. Gnd. pins: 3, 4, 5, 6, 7, 10, 11, 15, 16.

1. For quality control procedures, see Table of Contents.
2. For environmental specifications, see Table of Contents.
3. For connector types and case mounting options, see case style outline drawing.
4. Prices and specifications subject to change without notice.
5. All models are licensed under U.S. Patent 3,426,298.

Power Splitter/Combiners

8 WAY–0°

10 KHz to 4.2 GHz



	MODEL NO.	FREQ. RANGE MHz	ISOLATION dB						INSERTION LOSS, dB Above 9dB						PHASE UNBALANCE Degrees			AMPLITUDE UNBALANCE dB			PRICE $	DISTRIBUTOR	
		f_L–f_U	L Typ.	L Min.	M Typ	M Min.	U Typ.	U Min.	L Typ.	L Max.	M Typ.	M Max.	U Typ.	U Max.	L Max.	M Max	U Max	L Max.	M Max.	U Max.	Qty. (1-9)	FACTORY	LOCAL
PSC-8 case C07	PSC-8-1	0.5-175	30	25	30	20	25	18	0.8	1.2	0.8	1.2	1.0	1.6	1.0	2.5	5.0	0.2	0.3	0.5	74.95	●	●
	■PSC-8-1-75	0.5-175	25	20	30	20	25	20	0.5	1.0	0.6	1.1	0.7	1.3	1.0	2.5	5.0	0.2	0.2	0.3	78.95	●	●
	PSC-8-6	0.01-10	40	20	40	25	28	23	0.3	0.7	0.5	1.0	0.6	1.1	1.0	2.5	4.0	0.1	0.2	0.3	93.95	●	●
PSC-8A case E10	PSC-8A-4	5-500	25	20	23	18	20	15	0.7	1.2	1.0	1.8	1.4	2.5	3.0	8.0	16.0	0.2	0.3	0.5	103.95	●	●
	■PSC-8A4-75	1-300	26	20	30	25	30	23	0.8	1.2	0.7	1.1	0.9	1.3	1.0	3.0	8.0	0.2	0.2	0.4	93.95	●	●
ZC8PD case AC186	ZC8PD-900	800-900			30	20					0.4	0.7				5			0.4		158.95	●	
ZFSC-8 case R29	ZFSC-8-1	0.5-175	30	25	30	20	25	18	0.8	1.2	0.8	1.2	1.0	1.6	1.0	2.5	5.0	0.2	0.2	0.3	99.95	●	
	■ZFSC-8-1-75	0.5-175	25	20	30	20	25	20	0.5	1.0	0.6	1.1	0.7	1.3	1.0	2.5	5.0	0.2	0.3	0.5	102.95	●	
	■ZFSC-82-75	10-900	35	17	23	17	20	15	0.6	0.9	0.9	1.6	1.6	2.7	2.0	4.0	10.0	0.2	0.5	1.2	139.95		
	■ZFSC-84-75	1-300	26	20	30	25	30	23	0.8	1.5	0.7	1.1	0.9	1.5	1.0	3.0	8.0	0.2	0.2	0.4	119.95	●	
	■ZFSC-8375	50-90	30	25	30	25	25	25	1.0	1.0	1.0	1.3	1.3	1.3	2.0	2.0	2.0	0.2	0.2	0.2	119.95	●	
	ZFSC-8-4	5-700	35	20	25	17	20	17	0.8	1.2	1.2	1.8	1.8	2.5	2.0	5.0	15.0	0.2	0.4	0.7	128.95	●	
	ZFSC-8-43	10-1000	23	20	25	20	26	20	1.0	1.6	1.4	1.8	2.1	2.9	5.0	10.0	20.0	0.2	0.4	0.7	138.95	●	
	ZFSC-8-6	0.01-10	35	20	40	25	35	25	0.3	0.7	0.2	0.6	0.3	0.7	1.0	2.0	3.0	0.1	0.2	0.3	109.95	●	
ZB8PD case Z40	ZB8PD-2	GHz 1-2	24	17	24	17	24	17	0.8	1.3	0.8	1.3	0.8	1.3			18	0.8	0.8	0.8	138.95	●	
	ZB8PD-4	2-4.2	23	16	23	16	23	16	0.8	1.8	0.8	1.8	0.8	1.8	10	10	10	0.9	0.9	0.9	138.95	●	

L=low range (f_L to 10 f_L) M=mid range (10f_L to $f_U/2$) U=upper range ($f_U/2$ to f_U)

NOTES:

- ■ Denotes 75 ohm models. 75 ohm BNC connectors are standard.
  VSWR: input 1.06:1 typical, 1.2:1 max.
  output 1.17:1 typical, 1.35:1 max
1. Matched power rating, ZB8PD, ZC8PD, ZC10PD (10W), all other models (1W). internal load dissipation, 0.62 watts, for all 10 and 12 way models, 0.87 watts.
2. Refer to Table of Contents for quality control procedures, environmental specifications, and absolute maximum ratings.
3. For connector types, see case style outline drawing.
4. Prices and specifications subject to change without notice.
5. ZFSC-8-6, PSC-8-6: below 0.1 MHz power handling decrease as to typically 15 dBm at 0.01 MHz, 23 dBm at 0.025 MHz, & 29 dBm at 0.05 MHz.

NSN GUIDE

MCL NO.	NSN	MCL NO.	NSN	MCL NO.	NSN	MCL NO.	NSN
ZFSC-8-1 (BNC)	5820-01-136-7244	ZFSC-8-1 (SMA)	6620-01-223-1235	ZFSC-8-43 (SMA)	6625-01-333-1125	ZFSC-8-1-75	5895-01-326-8664

pin connections

see case style outline drawing

Series	Sum Port	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Case Ground	Do Not Use
PSC-8	2	1	5	9	13	16	12	8	4					3,6,7,14,15	10,11
*PSC-8A	29	7	16	31	24	9	2	26	17					All other pins	
PSC-10-1	29	7	16	31	24	9	2	26	17	4	5			All other pins	15
**PSC-12-1	5	7	8	1	2	31	32	25	26	22	30	19	27	All other pins	11,14,21

*Pins 4, 5 and 15 must be grounded externally for PSC-8A-4. Pin 15 must be grounded externally for PSC-8A4-75

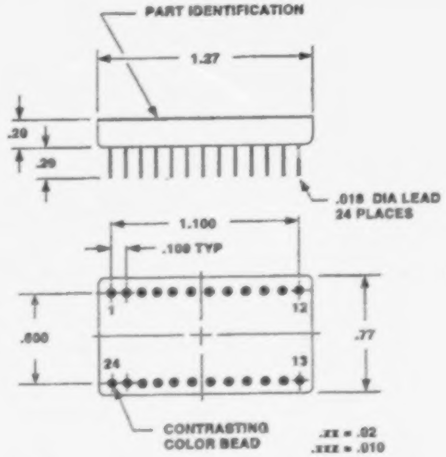
**Pin 4 must be grounded externally.

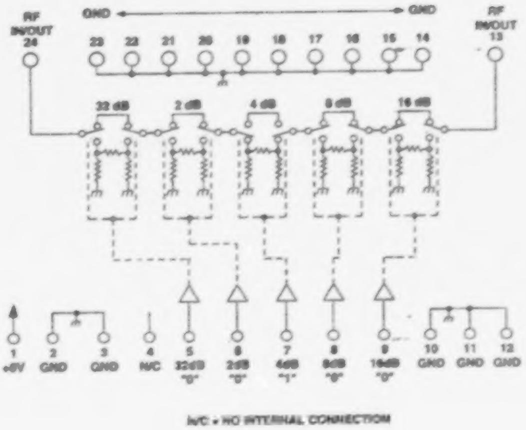
MODEL NO.
DA0857

GaAs 5 Section Attenuator

FEATURES

- 10 - 1000 MHz
- 1 mA, +5 VDC
- 2 dB LSB, 62 dB Range
- 38 nSec Switching Speed
- 12 nSec Transition Time
- TTL Control
- Small 24 Pin DIP
- See DA0757 For Surface Mount Version

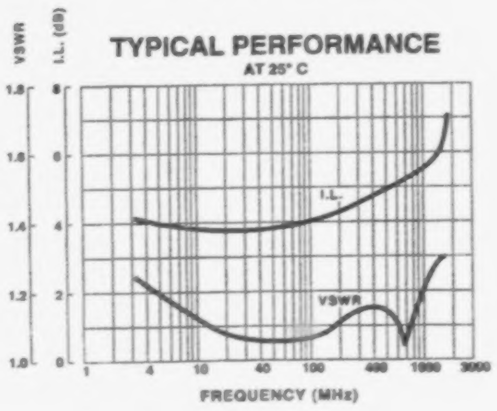

PART IDENTIFICATION
1.27
.20
.20
.018 DIA LEAD
24 PLACES
1.100
.100 TYP
1
12
24
13
.600
.77
CONTRASTING
COLOR BEAD
.xx = .02
.xxx = .010


RF
IN/OUT
24
GND
GND
RF
IN/OUT
13
23
22
21
20
19
18
17
16
15
14
32 dB
2 dB
4 dB
8 dB
16 dB
1
+5V
2
GND
3
GND
4
N/C
5
32dB
"0"
6
2dB
"0"
7
4dB
"1"
8
8dB
"0"
9
16dB
"0"
10
GND
11
GND
12
GND

N/C = NO INTERNAL CONNECTION

TYPICAL PERFORMANCE

AT 25° C



GUARANTEED PERFORMANCE

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
OPERATING FREQUENCY	10		1000	MHz	
DC CURRENT		1	5	mA	AT +5 VDC SUPPLY
CONTROL TYPE		TTL			5 LINES LOGIC "0" = THRU LOGIC "1" = ATTENUATION
CONTROL CURRENT HIGH LOW		0 0	±40 ±40	µA µA	VIH = +3.0V VIL = +0.5V
INSERTION LOSS		4.0 5.6	5.2 7.0	dB dB	10 - 100 MHz 100 - 1000 MHz
ATTENUATION LSB RANGE ACCURACY	0	2	62	dB dB dB	2, 4, 8, 16, 32 ± (0.25 dB +2% OF ATTEN. SETTING IN dB)
VSWR		1.2/1	1.4/1		
IMPEDANCE		50		OHMS	
SWITCHING SPEED		38	50	nSEC	50% TTL TO 90% / 10% RF
TRANSITION (RISE/FALL) TIME		12		nSEC	90% / 10% OR 10% / 90% RF
SWITCHING (VIDEO) TRANSIENTS		120		mV	PEAK VALUE
INTERCEPT POINTS, 2ND 3RD		+65 +44		dBm dBm	70 MHz / 50 MHz 25 MHz / 50 MHz
RF POWER OPERATE NO DAMAGE		+13	+10 +27	dBm dBm	0.1 dB COMPRESSION
OPERATING TEMPERATURE	-55	+25	+125	°C	TA

DAICO Contact Report

Page 1 of 1

TO

ATTN:

RE:

FAX

PROGRAM:

☐ PROPOSAL ☐ CONTRACT IN HOUSE

DATE: 9/23/92

CUSTOMER: Applied Silicon

CONTACT: John Curnow

PHONE: 613-592-0990 FAX: 613-592-0989

ADDRESS:

DETAILS:

Dear Mr. Curnow:

I am pleased to provide you with data on the DA0857 attenuator. The following is the typical phase change over attenuation at 60MHz:

Attn	ϕ
Thru	Ref
2	+0.2°
4	+0.2°
6	+0.4°
8	+0.5'
14	+1.0°
16	+0.7°
30	+1.5°
32	+1.0
62	+2.0

Please feel free to call me if you have any questions.

Regards,

ORIGINATOR

CC RD Associates (FAX #62)

DAICO INDUSTRIES, INC.
2453 East Del Amo Boulevard
Rancho Dominguez, CA 90220
310/631-1143 · FAX 310/631-8078

Signetics

Linear Products

NE/SA5204
Wide-band High-Frequency Amplifier

Product Specification

DESCRIPTION

The NE/SA5204 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ± 0.5dB from DC to 200MHz. The −3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204 operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204 is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204 solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

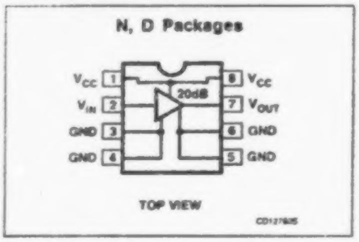
No external components are needed other than AC-coupling capacitors because the NE/SA5204 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204s in series as required, without any degradation in amplifier stability.

FEATURES

- **Bandwidth (min.)**
  200 MHz, ± 0.5dB
  350 MHz, − 3dB
- **20dB insertion gain**
- **4.8dB (6dB) noise figure**
  $Z_O = 75\Omega$ ($Z_O = 50\Omega$)
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface-mount package available**
- **Cascadable**

PIN CONFIGURATION



APPLICATIONS

- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broadband LANs**
- **Networks**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5204N
	−40 to +85°C	SA5204N
8-Pin Plastic SO package	0 to +70°C	NE5204D
	−40 to +85°C	SA5204D

Wide-band High-Frequency Amplifier NE/SA5204

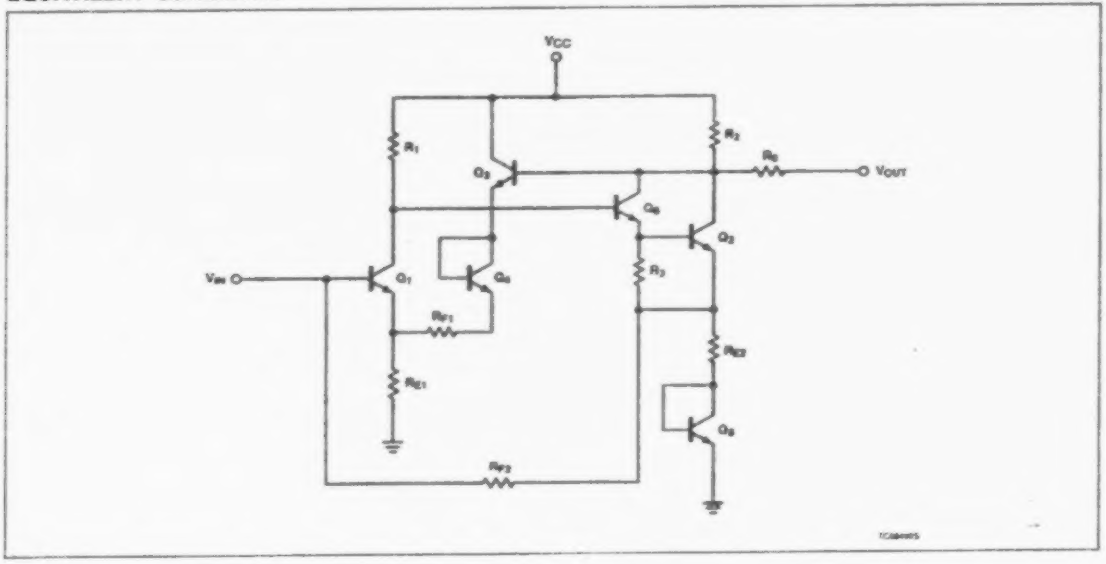
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range NE grade SA grade	 0 to +70 -40 to +85	 °C °C
P_{DMAX}	Maximum power dissipation[1, 2] T_A = 25°C (still-air) N package D package	 1160 780	 mW mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	-55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:

1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C.
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



Wide-band High-Frequency Amplifier

NE/SA5204

DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, Z_S = Z_L = Z_O = 50Ω and T_A = 25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	24	31	mA
S21	Insertion gain	f = 100MHz, over temperature	16	19	22	dB
S11	Input return loss	f = 100MHz		25		dB
		DC – 550MHz		12		dB
S22	Output return loss	f = 100MHz		27		dB
		DC – 550MHz		12		dB
S12	Isolation	f = 100MHz		–25		dB
		DC – 550MHz		–18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f = 100MHz		4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0		dB
	Saturated output power	f = 100MHz		+7.0		dBm
	1dB gain compression	f = 100MHz		+4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+24		dBm
t_R	Rise time			5		ps
	Propagation delay			5		ps

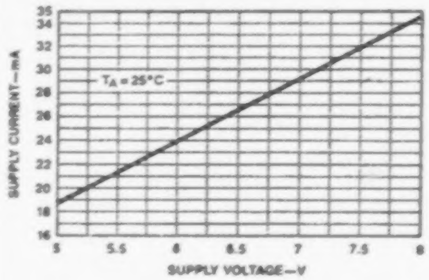


Figure 1. Supply Current vs Supply Voltage

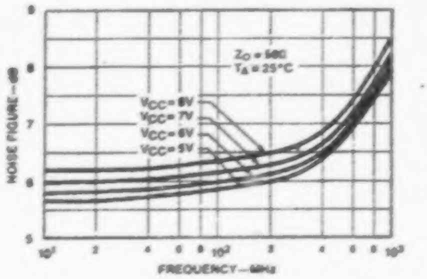


Figure 2. Noise Figure vs Frequency

PHASE SHIFTERS

FREQUENCY RANGE: 1-500 MHz

STANDARD MODELS:

PACKAGE	OUTLINE	PIN-OUT (See Below)	MODEL PREFIX	10% BANDWIDTH								OCTAVE	
FREQUENCY (MHz)				20	30	40	60	70	113	140	160	80-160	100-200
Flatpack	115	1	PF	-109	-101	-120	-102	-104	-105	-106	-107	-122	-123
Plug-In	124	2	PP	-909	-901	-920	-902	-904	-905	-906	-907	-922	-923
SMA	110	3	PK	-709S	-701S	-720S	-702S	-704S	-705S	-706S	-707S	-722S	-723S

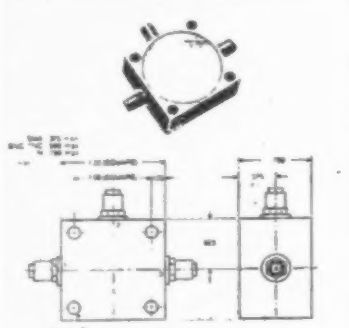
* Contact the factory for other frequency requirements

BASIC SPECIFICATIONS

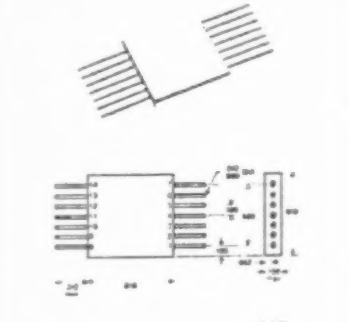
	BANDWIDTH 10%	OCTAVE
Insertion Loss (Max)	1.5 dB	2.0 dB
(Typ)	1.2 dB	1.5 dB
Phase Shift Range:	180°,Min	
Control Voltage:	0 to +30V	
Control Bandwidth:	DC-50 KHz	
VSWR:	1.7:1, Max	
Input Power:	-10dBm,Max	

PIN-OUT TABLE

	INPUT	OUTPUT	CONTROL	CASE GND
#1	14	7	1,8	All Other
#2	1	13	4	All Other
#3	1	3	2	-



110



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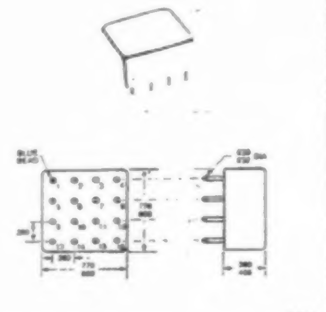

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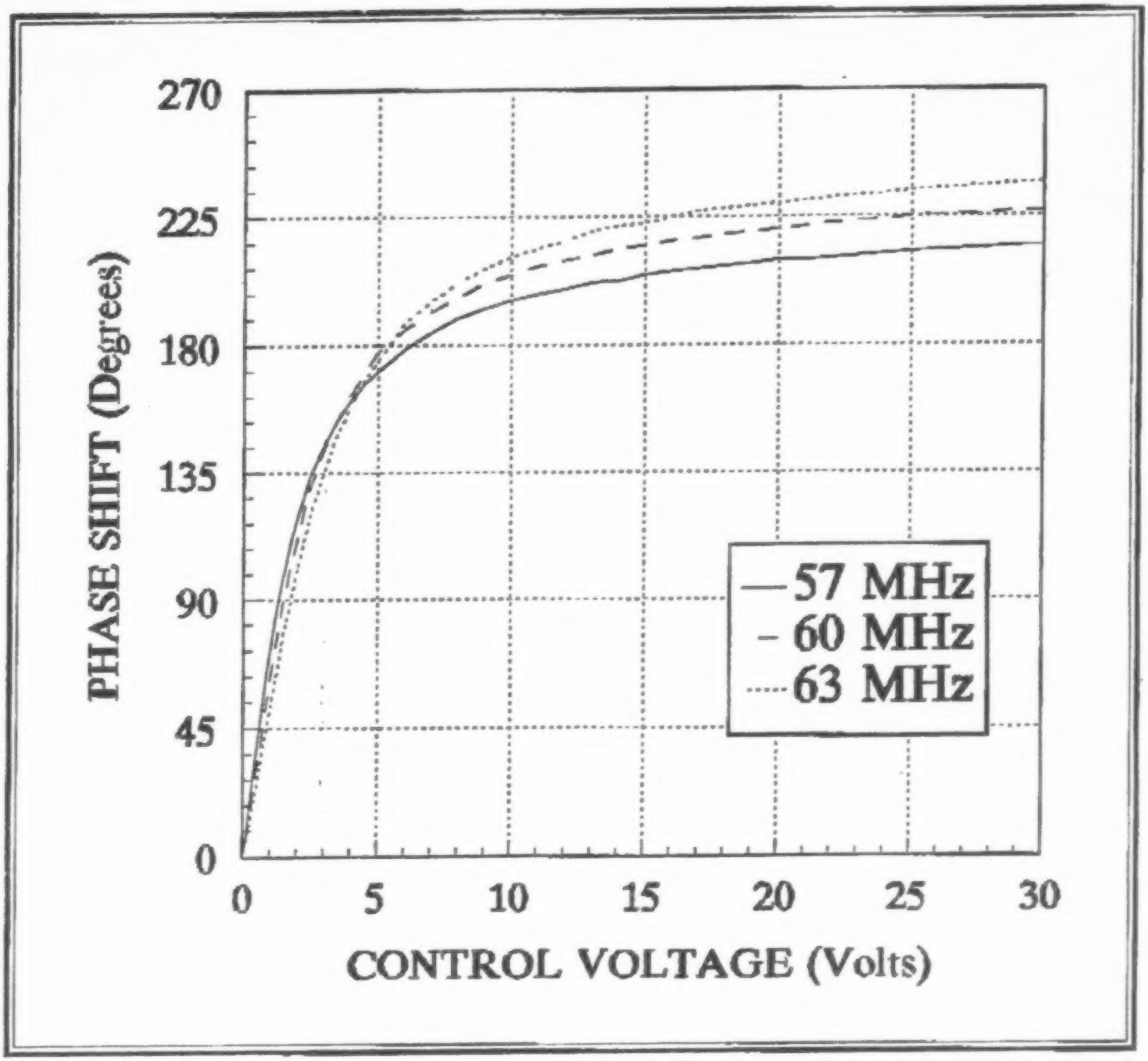
SYNERGY®
MICROWAVE CORPORATION

PP-902
TYPICAL PEROFRMANCE PLOTS



12 bit DAC 0 → 10 V output

SYNERGY
MICROWAVE CORPORATION

© 1992

∴ set all to ~ 1V
→ assume linear [0, 3] V

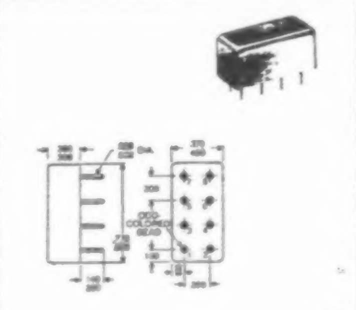
POWER DIVIDERS

0° : 3-WAY

FREQUENCY RANGE (MHz)	ISOLATION (dB)			INSERTION LOSS (dB)			PHASE UNBALANCE (Degrees)			AMPLITUDE UNBALANCE (dB)			OUTL. DWG.	PIN-OUT (See Below)	MODEL
LF-HF	LB TYP/MIN	MB TYP/MIN	UB TYP/MIN	LB TYP/MAX	MB TYP MAX	UB TYP MAX	LB MAX.	MB MAX.	UB MAX.	LB MAX.	MB MAX.	UB MAX.			
1-300	40/25	35/30	25/20	.20/0.5	.35/0.8	.50/1.0	3	3	4	.25	.25	.25	125	1	DCF-1L2
0.01-30	35/30	40/25	30/25	.25/.45	.15/.45	.45/.75	1	2	4	0.2	0.3	0.4	102	2	DCP-2A1
1-200	45/30	40/30	40/25	0.6/1.0	0.4/0.7	0.6/1.0	1	2	4	.15	0.2	0.3	102	2	DCP-2B2
1-200	35/23	35/25	35/25	0.6/1.0	0.3/0.7	0.6/1.0	2	3	4	.15	0.2	0.3	102	2	DCP-2C2 ■
5-500	25/20	31/15	25/15	0.4/0.8	0.4/1.4	0.8/1.4	6	6	10	0.1	0.3	0.6	102	3	DCP-2B3
1-200	45/30	48/35	37/30	0.25/0.5	.35/0.6	.35/0.6	1	3	5	0.1	0.2	0.2	113	4	DCK-7K2*
1-500	30/20	30/20	25/18	0.4/0.75	0.5/0.9	0.8/1.2	2	3	4	0.2	0.3	0.4	113	4	DCK-7J2*
2-750	30/20	30/20	25/18	0.4/0.75	0.5/1.0	1.0/1.6	3	5	7	0.2	0.3	0.5	113	4	DCK-7D3*

* Select Connector suffix: "B" = BNC, "S" = SMA, "N" = Type N, "T" = TNC
■ 75 Ohm Model
Power Rating (All Models) = 1 Watt, max

LB = LF to 10 LF
MB = 10 LF to HF/2
UB = HF/2 to HF



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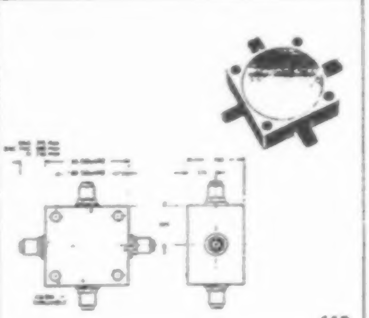

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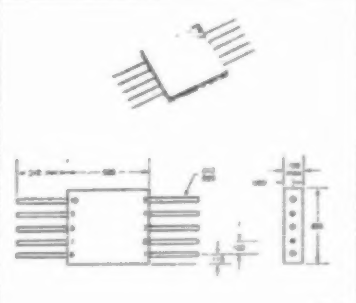
PIN-OUT TABLE

	INPUT	OUTPUT	CASE GROUND
#1	8	1,3,5	2,4,6,7,9
#2	6	1,2,5	3,4,7,8
#3	1	5,7,8	2,3,4,6
#4	1	2,3,4	-



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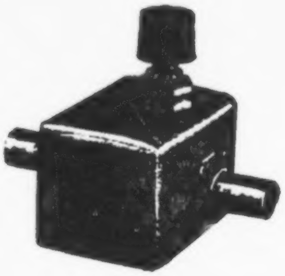
MANUAL VARIABLE ATTENUATORS

MODELS VA-422/423
VA-424/425

DC-500 MHz



DESCRIPTION

Lorch Electronics Variable Attenuators Models VA-422/423 and VA-424/425 are miniature components which may be adjusted manually by mechanical rotation to provide a useful range of smoothly variable attenuation over the frequency range DC to 500 MHz with low VSWR and low minimum insertion loss. Models VA-424/425 are smaller versions of Models VA-422/423 which feature the same electrical performance as the corresponding larger units.

The variable attenuators are ideal for applications where the gain of one or more channels must be set or equalized with precision. Models VA-422 and VA 424 are packaged with pins for PC board mounting, the control shaft being equipped with a screw driver slot and restrained by a shaft locking device. Models VA-423 and VA-425 have RF connectors and are provided with a manual knob adjustment.

Models VA-422 and VA-424 are intended primarily for chassis mounting within equipment where an initial setting will remain untouched except for an occasional readjustment. Models VA-423 and VA-425 are used in applications requiring frequent manual adjustment as is the case, for example, when they are front panel mounted.

Two frequency ranges are available in each configuration. Models VA-422A/423A and VA-424A/425A cover the frequency range from DC to 250 MHz; Models VA-422B/423B and VA-424B/425B are optimized for 250 to 500 MHz.

These attenuators use resistive network elements and thus cause no signal distortion. They are carefully compensated for wide bandwidth and are highly stable with time, humidity and temperature. They will remain at a preset attenuation value for a long period of time.

PERFORMANCE DATA

PC VERSION		CONNECTOR VERSION		FREQUENCY RANGE (MHz)	ATTENUATION RANGE	MINIMUM INSERTION LOSS	RESOLUTION	IMPEDANCE	VSWR
MODEL NO.	FIG.	MODEL NO.	FIG.						
VA-422A	1	VA-423A	2 NOTE 3	DC-250	0-25 dB to 100 MHz	0.3 dB to 100 MHz	0.1 dB	50 ohms*	1.2:1 to 100 MHz
					0-15 dB to 250 MHz	0.9 dB to 250 MHz			1.3:1 to 250 MHz
VA-424A	3	VA-425A	4	DC-250	0-25 dB to 100 MHz	0.3 dB to 100 MHz	0.1 dB	50 ohms*	1.2:1 to 250 MHz
					0-15 dB to 250 MHz	0.9 dB to 250 MHz			1.3:1 to 250 MHz
VA-422B	1	VA-423B	2 NOTE 3	250-500	0-10 dB	1.5 dB to 400 MHz	0.1 dB	50 ohms*	1.3:1
						2.2 dB to 500 MHz			
VA-424B	3	VA-425B	4	250-500	0-10 dB	1.5 dB to 400 MHz	0.1 dB	50 ohms*	1.3:1
						2.2 dB to 500 MHz			

NOTES:
1. Temperature Range: −55°C to +105°C.
2. Maximum R.F. input power (all models) 1 watt −55°C to +55°C; 0.5 watt +55°C to +75°C; 0.25 watt +75° C to +105°C.
3. BNC connectors are standard. SMA or TNC connectors may be obtained by adding -S or -T, e.g., VA-423A-75-T.

* For 75 ohms add suffix -75 to model designation.

ANALOG DEVICES

Wideband, High Output Current, Fast Settling Op Amp

AD842

FEATURES

AC PERFORMANCE

Gain Bandwidth Product: 80 MHz (Gain = 2)
Fast Settling: 100 ns to 0.01% for a 10 V Step
Slew Rate: 375 V/µs
Stable at Gains of 2 or Greater
Full Power Bandwidth: 6.0 MHz for 20 V p-p

DC PERFORMANCE

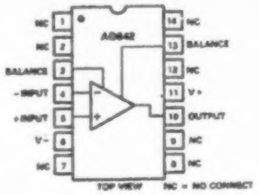
Input Offset Voltage: 1 mV max
Input Offset Drift: 14 µV/°C
Input Voltage Noise: 9 nV/$\sqrt{Hz}$ typ
Open-Loop Gain: 90 V/mV into a 500 Ω Load
Output Current: 100 mA min
Quiescent Supply Current: 14 mA max

APPLICATIONS

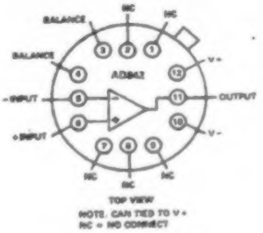
Line Drivers
DAC and ADC Buffers
Video and Pulse Amplifiers
Available in Plastic DIP and Hermetic Metal Can, Hermetic Cerdip Packages and in Chip Form
MIL-STD-883B Parts Available

AD842 CONNECTION DIAGRAMS

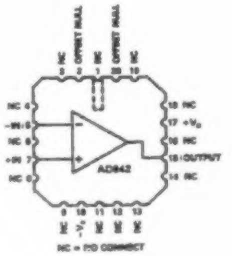
Plastic DIP (N) Package
and
Cerdip (Q) Package


NC 1
NC 2
BALANCE 3
−INPUT 4
+INPUT 5
V− 6
NC 7
14 NC
13 BALANCE
12 NC
11 V+
10 OUTPUT
9 NC
8 NC
AD842
TOP VIEW
NC = NO CONNECT

LCC (E) Package


BALANCE
NC
NC
BALANCE
V+
AD842
−INPUT
OUTPUT
+INPUT
V−
NC
NC
NC
1
2
3
4
5
6
7
8
9
10
11
12
TOP VIEW
NOTE: CAN TIED TO V+
NC = NO CONNECT

TO-8 (H)
Package


NC 3
OFFSET NULL 2
NC 1
OFFSET NULL 20
NC 19
NC 4
−IN 5
NC 6
+IN 7
NC 8
18 NC
17 +V
16 NC
15 OUTPUT
14 NC
AD842
9 NC
10 −V
11 NC
12 NC
13 NC
NC = NO CONNECT

PRODUCT DESCRIPTION

The AD842 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840 which is stable at a gain of 10 or greater and the AD841 which is unity-gain stable. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 80 MHz gain bandwidth, the AD842 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 100 ns for a 10 volt step.

The AD842 also offers a low quiescent current of 13 mA, a high output current drive capability (100 mA minimum), a low input voltage noise of 9 nV$\sqrt{Hz}$ and a low input offset voltage (1 mV maximum).

The 375 V/µs slew rate of the AD842, along with its 80 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD842 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD842 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD842 make it ideal for DAC and ADC buffers amplifiers, lines drivers and all types of video instrumentation circuitry.
2. The AD842 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth; performance previously available only in hybrids.
3. Laser-wafer trimming reduces the input offset voltage of 1 mV max, thus eliminating the need for external offset nulling in many applications.
4. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where the circuit gain will be 2 or greater.
5. The AD842 is an enhanced replacement for the HA2542.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD842J			AD842K			AD842S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]			0.5	1.5		0.3	1.0		0.5	1.5	mV
	T_{min}–T_{max}			2.5			1.5			3.5	mV
Offset Drift			14			14			14		μV/°C
INPUT BIAS CURRENT			4.2	8		3.5	5		4.2	8	μA
	T_{min}–T_{max}			10			6			12	μA
Input Offset Current			0.1	0.4		0.05	0.2		0.1	0.4	μA
	T_{min}–T_{max}			0.5			0.3			0.6	μA
INPUT CHARACTERISTICS											
Input Resistance	Differential Mode		100			100			100		kΩ
Input Capacitance			2.0			2.0			2.0		pF
INPUT VOLTAGE RANGE											
Common Mode		± 10			±10			±10			V
Common-Mode Rejection	V_{CM} = ±10 V	86	115		90	115		86	115		dB
	T_{min}–T_{max}	80			86			80			dB
INPUT VOLTAGE NOISE	f = 1 kHz		9			9			9		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		28			28			28		μV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	40	90		50	90		40	90		V/mV
	T_{min}–T_{max}	20			25			20			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	± 10			±10			±10			V
Current	V_{OUT} = ±10 V	100			100			100			mA
	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV		80			80			80		MHz
Full Power Bandwidth[2]	V_O = 20 V p-p										
	R_{LOAD}≥500 Ω	4.7	6		4.7	6		4.7	6		MHz
Rise Time[3]	A_{VCL} = −2		10			10			10		ns
Overshoot[3]	A_{VCL} = −2		20			20			20		%
Slew Rate[3]	A_{VCL} = −2	300	375		300	375		300	375		V/μs
Settling Time[3]	10 V Step										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
Differential Gain	f = 4.4 MHz		0.015			0.015			0.015		%
Differential Phase	f = 4.4 MHz		0.035			0.035			0.035		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current			13	14		13	14		13	14	mA
	T_{min}–T_{max}			16			16			19	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V	86	100		90	105		86	100		dB
	T_{min}–T_{max}	80			86			80			dB
TEMPERATURE RANGE											
Rated Performance[4]		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[5]											
Plastic (N-14)			AD842JN			AD842KN					
Cerdip (Q-14)			AD842JQ			AD842KQ			AD842SQ		
TO-8 (H-12A)			AD842JH			AD842KH			AD842SH		
LCC[6] (E-20A)									AD842SE		
J and S Grade Chips Also Available											

NOTES

[1] Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2] FPBW Slew Rate/2π V_{PEAK}.

[3] Refer to Figures 22 and 23.

[4] "S" grade T_{min} and T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

[5] See Section 20 for package outline information.

[6] Contact factory for availability.

All min and max specifications are guaranteed. Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ANALOG DEVICES

450 V/μs, Precision, Current-Feedback Op Amp

AD846

FEATURES

AC PERFORMANCE
Small Signal Bandwidth: 80 MHz ($A_V = -1$)
Slew Rate: 450 V/μs
Full Power Bandwidth: 6.8 MHz at 20 V p-p, $R_L = 500\ \Omega$
Fast Settling: for 10 V Step: 110 ns to 0.01%, 80 ns to 0.1%
Differential Gain: <0.01% @ 4.4 MHz
Differential Phase: <0.028° @ 4.4 MHz
Total Harmonic Distortion (THD): 0.0005% @ 100 kHz
Open-Loop Transimpedance: 200 MΩ
Input Voltage Noise: 2 nV/$\sqrt{Hz}$

DC PERFORMANCE
Input Offset Voltage: 75 μV max (B Grade)
Input Offset Drift: 3.5 μV/°C max (B Grade)
Quiescent Supply Current: 6.5 mA max

APPLICATIONS
High Speed DAC Buffers
Multiflash ADC Error Amplifiers
Flash ADC Buffers
Coaxial Cable Drivers
High Performance Audio Circuitry
Available in Plastic Mini-DIP, Hermetic Cerdip, and Hermetic Metal Can Packages
MIL-STD-883B Parts Available

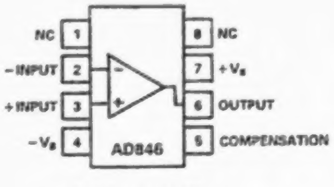
PRODUCT DESCRIPTION

The AD846 is a monolithic, very high speed operational amplifier offering high performance. Although technically classed as a current-feedback or transimpedance amplifier, it may be used in much the same way as traditional op amps while providing significant performance benefits. Employing Analog Devices' junction isolated complementary bipolar (CB) process, the AD846 achieves true "12-bit" (0.01%) precision on critical ac and dc parameters, a level of performance unmatched by amplifiers fabricated using either the dielectrically isolated (DI) or other bipolar processes.

The AD846 offers significant advantages over conventional high speed operational amplifiers. It maintains a nearly constant bandwidth and settling time to 0.01% over a wide range of closed-loop gains. This makes the AD846 ideal for amplifying the residue in multiple-pass analog-to-digital converters.

AD846 CONNECTION DIAGRAM

Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package
Top View



NC = NO CONNECT

Other advantages include: low input errors and high open-loop transresistance (200 MΩ) into a 500 Ω load, ensuring true 12-bit dc accuracy for closed-loop gains from −1 to gains greater than −100. This combination of ac and dc performance makes the AD846 an excellent choice for buffering precision high speed DACs and flash ADCs.

The AD846 is available in three performance grades. The AD846A and AD846B are rated over the industrial temperature range of −40°C to +85°C. The AD846S is rated over the full military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C.

Extended reliability PLUS screening is available specified over the commercial temperature range. PLUS screening includes 168 hour burn-in as well as other environmental and physical tests. The AD846 is available in two types of 8-pin package: plastic mini-DIP and hermetic cerdip. "A" and "S" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD846 achieves settling times of 110 ns to 0.01% for gains of −1 to −10, with a 450 V/μs slew rate, while consuming only 5 mA of supply current.
2. For closed-loop gains of −1 to −100, the high speed performance of the AD846 is achieved without sacrificing full 12-bit dc precision.
3. The AD846 is well suited to line driver and video buffer applications where the properties of low distortion and high slew rate are required.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD846A			AD846B			AD846S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]											
Initial			25	200		25	75		25	200	µV
T_{min}–T_{max}			50	350		50	125		100	350	µV
vs. Temperature			0.8	5		0.8	3.5		1	5.5	µV/°C
vs. Supply (PSSR)	5 V–18 V[2]										
Initial		110	125		120	125		110	125		dB
T_{min}–T_{max}		110	120		116	120		94	116		dB
vs. Common Mode	V_{CM} = ±10 V										
Initial		110	125		120	125		110	125		dB
T_{min}–T_{max}		110	120		116	120		94	116		dB
INPUT BIAS CURRENT[3]											
−Input Bias Current											
Initial			150	450		100	250		150	450	nA
T_{min}–T_{max}			450	1200		400	750		1000	1500	nA
vs. Temperature			6	20		6	17		9	20	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			9	15		9	10		9	15	nA/V
T_{min}–T_{max}			11	20		11	15		11	25	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	10		3	5		5	10	nA/V
T_{min}–T_{max}			5	15		3	7		5	20	nA/V
+Input Bias Current											
Initial			3	15		3	5		3	15	µA
T_{min}–T_{max}			4	20		4	7		5	20	µA
vs. Temperature			15	80		15	45		15	80	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			5	15		5	10		5	15	nA/V
T_{min}–T_{max}			5	20		5	15		5	20	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	15		3	10		5	15	nA/V
T_{min}–T_{max}			5	15		3	10		5	20	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
−Input			50			50			50		Ω
+Input			10			10			10		kΩ
Input Capacitance											
−Input			2			2			2		pF
+Input			2			2			2		pF
INPUT VOLTAGE RANGE Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	F = 1 kHz		2			2			2		nV/√Hz
Input Current Noise											
−Input	1 kHz		20			20			20		pA/√Hz
+Input	1 kHz		6			6			6		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT} = ±10 V R_{LOAD} = 500 Ω	100	200		150	200		100	200		MΩ
	T_{min}–T_{max}	50			75			50			MΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500 Ω	±10			±10			±10			V
Current	Short Circuit		65			65			65		mA
Output Resistance	Open Loop		16			16			16		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth (−3dB)	A_V = −1 R_F = 1 k		80			80			80		MHz
	A_V = −10 R_F = 875 Ω		31			31			31		MHz
	A_V = −30 R_F = 875 Ω		15			15			15		MHz
Full Power Bandwidth[4]	V_{OUT} = 20 V p-p R_L = 500 Ω		6.8			6.8			6.8		MHz
Rise Time	A_V = −1		10			10			10		ns
Overshoot	A_V = −1		20			20			20		%
Slew Rate	A_V = −1		450			450			450		V/µs
Settling Time											
10 V Step, A_V = −1	to 0.1%		80			80			80		ns
	to 0.01%		110			110			110		ns
TOTAL HARMONIC DISTORTION[5]	F = 100 kHz		0.0005			0.0005			0.0005		%

ANALOG DEVICES

µP-Compatible Multiplying Quad 12-Bit D/A Converters

AD394/AD395

FEATURES

- **Four Complete 12-Bit CMOS DACs with Buffer Registers**
- **Linearity Error ± 1/2LSB T_{min}-T_{max} (AD394, AD395K,T)**
- **Factory-Trimmed Gain and Offset**
- **Precision Output Amplifiers for V_{OUT}**
- **Full Four Quadrant Multiplication per DAC**
- **Monotonicity Guaranteed Over Full Temperature Range**
- **Fast Settling: 15µs Max to ± 1/2LSB**
- **Available to MIL-STD-883 (See ADI Military Catalog)**

PRODUCT DESCRIPTION

The AD394 and AD395 contain four 12-bit, high-speed, low power, voltage output multiplying digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit CMOS DAC chip which reduces chip count and provides high reliability. The AD394 and AD395 both are ideal for systems requiring digital control of many analog voltages where board space is at a premium and low power consumption a necessity. Such applications include automatic test equipment, process controllers, and vector stroke displays.

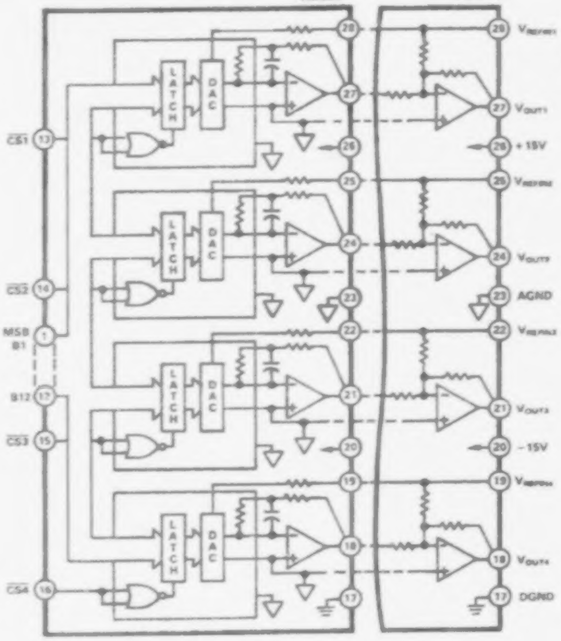
Both the AD394 and the AD395 are laser-trimmed to ± 1/2LSB max differential and integral linearity (AD394, AD395K,T) and full scale accuracy of ± 0.05 percent at 25°C. The high initial accuracy is made possible by the use of precision laser trimmed thin-film scaling resistors.

The individual DAC registers are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control pins. These control signals allow any combination of the DAC select matrix to occur (see Table III). Once selected, the DAC is loaded with a single 12-bit wide word. The 12-bit parallel digital input interfaces to most 12- and 16-bit bus systems.

The AD394 outputs (V_{REFIN} = + 10V) provide a ± 10V bipolar output range with positive-true offset binary input coding. The AD395 outputs (V_{REFIN} = − 10V) provide a 0V to + 10V unipolar output range with straight binary input coding.

Both the AD394 and the AD395 are packaged in a 28-lead ceramic package and are available for operation over the 0 to + 70°C and − 55°C to + 125°C temperature range.

AD394/AD395 FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

1. The AD394, AD395 offer a dramatic reduction in printed circuit board space in systems using multiple DACs.
2. The use of CMOS DACs provides low power consumption.
3. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
4. The output voltage is trimmed to a full scale accuracy of ± 0.05%. Settling time to ± 1/2LSB is 15 microseconds maximum.
5. Maximum gain TC of 5ppm/°C is achievable by both the AD394 and the AD395.
6. The monolithic CMOS DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
7. The 28-pin double-width hybrid package provides extremely high functional density.
8. Two or four quadrant multiplication can be achieved simply by applying the appropriate input voltage signal to the selected DAC's reference (V_{REFIN}).
9. Both the AD394S,TD and AD395S,TD feature guaranteed accuracy and linearity over the − 55°C to + 125°C temperature range.

SPECIFICATIONS (T_A = +25°C, V_{REFIN} = 10V, V_S = ±15V unless otherwise specified)

Model	AD394JD/SD[1] AD395JD/SD			AD394KD/TD[1] AD395KD/TD			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Pins 1-16)[2]							
TTL or 5 Volt CMOS Compatible							
Input Voltage							
Bit ON (Logic "1")	+2.4		+5.5	+2.4		+5.5	V
Bit OFF (Logic "0")	0		+0.8	0		+0.8	V
Input Current		±4	±40		±4	±40	µA
RESOLUTION			12			12	Bits
OUTPUT							
Voltage Range[3]							
AD394		$\pm V_{REFIN}$			$\pm V_{REFIN}$		V
AD395		0V to $-(V_{REFIN})$			0V to $-(V_{REFIN})$		V
Current	5			5			mA
STATIC ACCURACY							
Gain Error		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Bipolar Zero (AD394)		±0.025			±0.012		% of FSR
Integral Linearity Error[5]		±1/4	±3/4		±1/8	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
TEMPERATURE PERFORMANCE							
Gain Drift			±10			±5	ppm FSR/°C
Offset Drift			±10			±5	ppm FSR/°C
Integral Linearity Error[5] T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
REFERENCE INPUTS							
Input Resistance	5		25	5		25	kΩ
Voltage Range	−11		+11	−11		+11	V
DYNAMIC PERFORMANCE							
Settling Time (to ±1/2LSB)							
V_{REFIN} = +10V, Change All Digital Inputs from +5.0V to 0V		10	15		10	15	µs
V_{REFIN} = 0 to 5V Step, All Digital Inputs = 0V		10	15		10	15	µs
Reference Feedthrough Error[6]							
AD395		5			5		mV p-p
AD394		See Figure 1			See Figure 1		
Digital-to-Analog Glitch Impulse[7]		250			250		nV-sec
Crosstalk							
Digital Input (Static)[8]		0.1			0.1		LSB
Reference[9]		2.0			2.0		mV p-p
POWER REQUIREMENTS							
Supply Voltage[10]	±13.5		±16.5	±13.5		±16.5	V
Current (All Digital Inputs 0V or +5V)							
$+V_S$		20	22		20	22	mA
$-V_S$		18	28		18	28	mA
Power Dissipation		570	750		570	750	mW
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1] AD394 and AD395 S and T grades are available to MIL-STD-883, Method 5008, Class B. See Analog Devices Military Catalog (1987) for proper part number and detail specification.

[2] Timing specifications appear in Table IV and Figure 5.

[3] Code tables and graphs appear on Theory of Operation page.

[4] FSR means Full Scale Range and is equal to 20V for a ±10V bipolar range and 10V for 0 to 10V unipolar range.

[5] Integral nonlinearity is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function.

[6] For AD395 (unipolar), DAC register loaded with 0000 0000 0000, V_{REFIN} = 20V p-p, 10kHz sinewave. For AD394 (bipolar), V_{REFIN} = 20V p-p, 60 and 400Hz.

[7] This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVs and is measured with V_{REFIN} = AGND.

[8] Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2kΩ load by means of varying the digital input code.

[9] Reference crosstalk is defined as the change in any one output as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} @ 10kHz into a 2kΩ load by means of varying the amplitude of the reference signal.

[10] The AD394 and the AD395 can be used with supply voltages as low as ±11.4V, Figure 10.

Specifications subject to change without notice.

ANALOG DEVICES

±10 Volt Precision Reference Series

AD2700/AD2701/AD2702

FEATURES

Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed -55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected
Available as /883B

PRODUCT DESCRIPTION

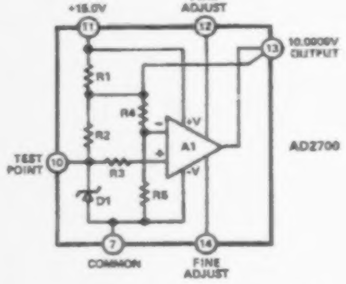
The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C.

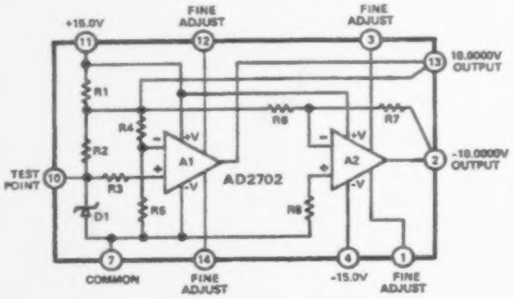
The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package. Both are often used with 52XX Series 12-bit A/D converters which require -10V external references for high accuracy over wide temperature ranges.

All three devices are offered in "J" and "L" grades for operation from -25°C to +85°C and "S" and "U" grades for the -55°C to +125°C temperature range. Screening to MIL-STD-883 is available for "S" and "U" grades of the AD2700 family.

AD2700 SERIES FUNCTIONAL BLOCK DIAGRAMS





PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature performance results in very high accuracy over the temperature range without external components. The AD2700/01/02 LD grades have a maximum output voltage error at 25°C of ±2.5mV with no external adjustments.
2. The performance of the AD2700 series is achieved by a well-characterized design and precise control over the manufacturing process.
3. The AD2700 series is well suited for a broad range of applications requiring an accurate, stable reference source such as high resolution data converters (12 or 14 bits), test and measurement systems and calibration standards.

Model	Output
AD2700	+10.000V
AD2701	-10.000V
AD2702	±10.000V

SPECIFICATIONS (max or min @ E_{IN} ±15V @ +25°C, $R_L = 2k\Omega$ unless otherwise noted)

MODEL	JD	LD	SD	UD
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	•	•	•
Power Dissipation @ +25°C – AD2700, 01	300mW	•	•	•
– AD2702	450mW	•	•	•
Operating Temperature Range	-25°C to +85°C	•	-55°C to +125°C	•••
Storage Temperature Range	-65°C to +150°C	•	•	•
Lead Temperature (soldering, 10s)	+300°C	•	•	•
Short Circuit Protection (to GND)	Continuous	•	•	•
OUTPUT VOLTAGE ERROR @ +25°C				
AD2700 10.000V	±0.005V	±0.0025V	•	••
AD2701 -10.000V	±0.005V	±0.0025V	•	••
AD2702 ±10.000V	±0.005V	±0.0025V	•	••
OUTPUT CURRENT[1] – @ +25°C	±10mA	•	•	•
(V_{IN} = ±13 to ±18V) over op. temp. range	±5mA	+5mA, -2mA	••	••
OUTPUT VOLTAGE ERROR – AD2700,01	10ppm/°C	3ppm/°C	••	••
(T_{min} to T_{max})[2]	±11.0mV	±4.3mV	±8mV	±5.5mV
AD2702	10ppm/°C	5ppm/°C	••	3ppm/°C
	±11.0mV	±5.5mV	±10.0mV	±5.5mV
LINE REGULATION				
V_{IN} = ±13.5 to ±16.5V	300µV/V	•	•	•
LOAD REGULATION				
0 to ±10mA	50µV/mA	•	•	•
OUTPUT RESISTANCE	0.05Ω	•	•	•
INPUT VOLTAGE, OPERATING	±13V to ±18V	•	•	•
QUIESCENT CURRENT – AD2700, 01	±14mA	•	•	•
– AD2702	+17mA, -4mA	•	•	•
NOISE				
(0.1 to 10Hz)	50µV p-p typ	•	•	•
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. (typ)	•	•	•
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV (min)	•	•	•
OFFSET ADJUST TEMP DRIFT EFFECT	±4µV/°C per mV of Adjust (typ)	•	•	•
PACKAGE OPTION[3,4]	DH-14C	DH-14C	DH-14C	DH-14C

NOTES
•Same as "JD" grade performance.
••Same as "LD" grade performance.
•••Same as "SD" grade performance.

[1] Specified with resistive load to common. Device not intended for use in driving a dynamic load.

[2] Output voltage error as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C. The box limits are noted below the drift values used to calculate the box.

[3] Analog Devices reserves the right to ship metal packages (outline DH-14B) in lieu of the standard ceramic packages for J and L grade parts.

[4] See Section 14 for package outline information.

Specifications subject to change without notice.

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LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and mininize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

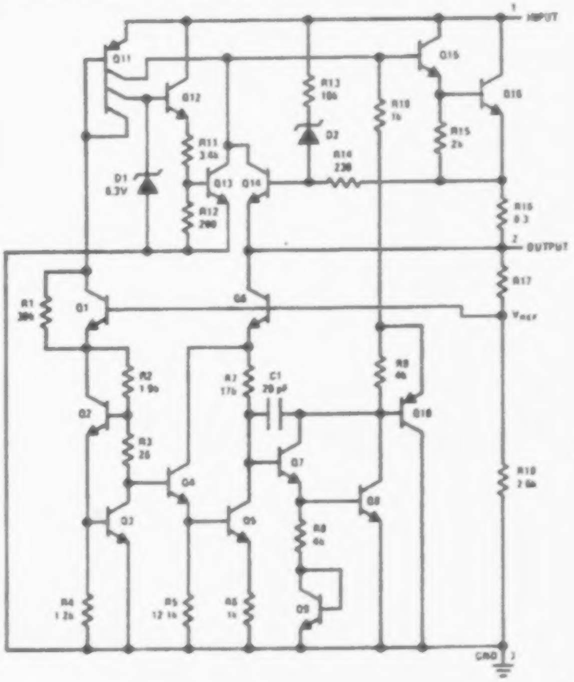
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

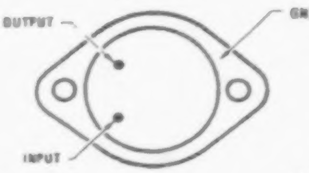
LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams



TL/H/7746-1

Metal Can Package
TO-3 (K)
Aluminum

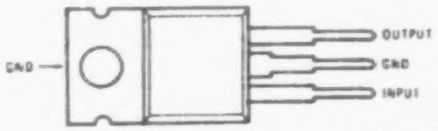


TL/H/7746-2

Bottom View

Order Number LM7805CK,
LM7812CK or LM7815CK
See NS Package Number KC02A

Plastic Package
TO-220 (T)



TL/H/7746-3

Top View

Order Number LM7805CT,
LM7812CT or LM7815CT
See NS Package Number T03B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-3 Package K	300°C
TO-220 Package T	230°C

Electrical Characteristics LM78XXC (Note 2) 0°C ≤ Tj ≤ 125°C unless otherwise noted.

Output Voltage				5V			12V			15V			Units
Input Voltage (unless otherwise noted)				10V			19V			23V			
Symbol	Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	Tj = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A		4.75		5.25	11.4		12.6	14.25		15.75	V
		$V_{MIN} \le V_{IN} \le V_{MAX}$			(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)		V
ΔV_O	Line Regulation	I_O = 500 mA	Tj = 25°C		3	50		4	120		4	150	mV
			ΔV_{IN}		(7 ≤ V_{IN} ≤ 25)			14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)		V
			0°C ≤ Tj ≤ +125°C			50			120			150	mV
			ΔV_{IN}		(8 ≤ V_{IN} ≤ 20)			(15 ≤ V_{IN} ≤ 27)			(18.5 ≤ V_{IN} ≤ 30)		V
		I_O ≤ 1A	Tj = 25°C			50			120			150	mV
			ΔV_{IN}		(7.5 ≤ V_{IN} ≤ 20)			(14.6 ≤ V_{IN} ≤ 27)			(17.7 ≤ V_{IN} ≤ 30)		V
			0°C ≤ Tj ≤ +125°C			25			60			75	mV
			ΔV_{IN}		(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)		V
ΔV_O	Load Regulation	Tj = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	mV
			250 mA ≤ I_O ≤ 750 mA			25			60			75	mV
		5 mA ≤ I_O ≤ 1A, 0°C ≤ Tj ≤ +125°C				50			120			150	mV
I_Q	Quiescent Current	I_O ≤ 1A	Tj = 25°C			8			8			8	mA
			0°C ≤ Tj ≤ +125°C			8.5			8.5			8.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	mA
		Tj = 25°C, I_O ≤ 1A				1.0			1.0			1.0	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$			(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)		V
		I_O ≤ 500 mA, 0°C ≤ Tj ≤ +125°C				1.0			1.0			1.0	mA
		$V_{MIN} \le V_{IN} \le V_{MAX}$			(7 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)		V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	I_O ≤ 1A, Tj = 25°C or	62	80		55	72		54	70		dB
			I_O ≤ 500 mA 0°C ≤ Tj ≤ +125°C	62			55			54			dB
		$V_{MIN} \le V_{IN} \le V_{MAX}$			(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)		V
R_O	Dropout Voltage	Tj = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz			8			18			19		mΩ
	Short-Circuit Current	Tj = 25°C			2.1			1.5			1.2		A
	Peak Output Current	Tj = 25°C			2.4			2.4			2.4		A
	Average TC of V_{OUT}	0°C ≤ Tj ≤ +125°C, I_O = 5 mA			0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	Tj = 25°C, I_O ≤ 1A			7.5		14.6			17.7			V

Note 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

Note 2: All characteristics are measured with capacitor across the input of 0.22 μF, and a capacitor across the output of 0.1μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

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LM79XX Series 3-Terminal Negative Regulators

General Description

The LM79XX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

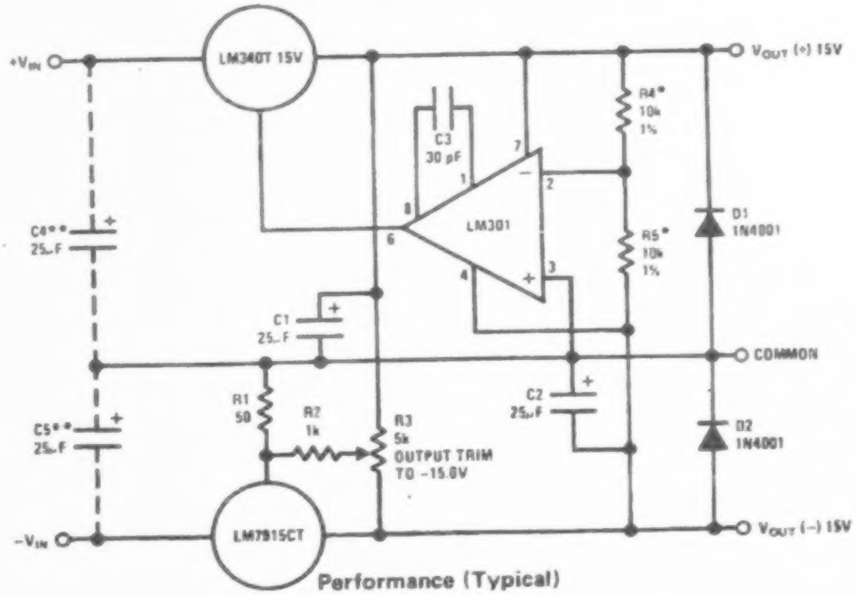
For applications requiring other voltages, see LM137 data sheet.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% preset output voltage

Typical Applications

± 15V, 1 Amp Tracking Regulators


+VIN
LM340T 15V
VOUT (+) 15V
C3
30 pF
R4*
10k
1%
7
1
2
8
6
LM301
3
4
C4**
25µF
R5*
10k
1%
D1
1N4001
C1
25µF
COMMON
C2
25µF
C5**
25µF
R1
50
R2
1k
R3
5k
OUTPUT TRIM
TO -15.0V
D2
1N4001
-VIN
LM7915CT
VOUT (−) 15V

TL/H/7340-1

Performance (Typical)

	(−15)	(+15)
Load Regulation at $\Delta I_L = 1A$	40 mV	2 mV
Output Ripple, $C_{IN} = 3000\ \mu F$, $I_L = 1A$	100 µVrms	100 µVrms
Temperature Stability	50 mV	50 mV
Output Noise $10\ Hz \le f \le 10\ kHz$	150 µVrms	150 µVrms

*Resistor tolerance of R4 and R5 determine matching of (+) and (−) outputs.

**Necessary only if raw supply filter capacitors are more than 3" from regulators.

Electrical Characteristics (Continued) Conditions unless otherwise noted: I_{OUT} = 500 mA, C_{IN} = 2.2 μF, C_{OUT} = 1 μF, 0°C ≤ T_J ≤ +125°C, Power Dissipation = 1.5W.

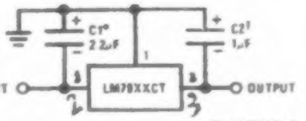
Part Number			LM7912C			LM7915C			Units
Output Voltage			12V			15V			
Input Voltage (unless otherwise specified)			−19V			−23V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_J = 25°C	−11.5	−12.0	−12.5	−14.4	−15.0	−15.6	V
		5 mA ≤ I_{OUT} ≤ 1A,	−11.4		−12.6	−14.25		−15.75	V
		P ≤ 15W		(−27 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)		V
ΔV_O	Line Regulation	T_J = 25°C, (Note 2)		5	80		5	100	mV
				(−30 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)		V
				3	30		3	50	mV
				−22 ≤ V_{IN} ≤ −16)			(−26 ≤ V_{IN} ≤ −20)		V
ΔV_O	Load Regulation	T_J = 25°C, (Note 2)		15	200		15	200	mV
		5 mA ≤ I_{OUT} ≤ 1.5A		15	200		15	200	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		5	75		5	75	mV
I_Q	Quiescent Current	T_J = 25°C		1.5	3		1.5	3	mA
ΔI_Q	Quiescent Current Change	With Line			0.5			0.5	mA
				(−30 ≤ V_{IN} ≤ −14.5)			(−30 ≤ V_{IN} ≤ −17.5)		V
		With Load, 5 mA ≤ I_{OUT} ≤ 1A			0.5			0.5	mA
V_n	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 Hz		300			375		μV
	Ripple Rejection	f = 120 Hz	54	70		54	70		dB
				(−25 ≤ V_{IN} ≤ −15)			(−30 ≤ V_{IN} ≤ −17.5)		V
	Dropout Voltage	T_J = 25°C, I_{OUT} = 1A		1.1			1.1		V
I_{OMAX}	Peak Output Current	T_J = 25°C		2.2			2.2		A
	Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0 C ≤ T_J ≤ 100°C		−0.8			−1.0		mV/°C

Note 1: For calculations of junction temperature rise due to power dissipation, thermal resistance junction to ambient (θ_{JA}) is 50°C/W (no heat sink) and 5°C/W (infinite heat sink).

Note 2: Regulation is measured at a constant junction temperature by pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account.

Typical Applications (Continued)

Fixed Regulator



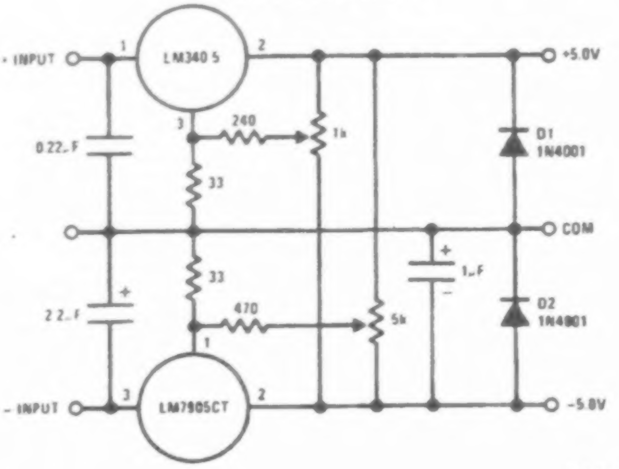
TL/H/7340-3

*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25 μF aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100 μF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

Dual Trimmed Supply



TL/H/7340-4

National Semiconductor Corporation

LM140L/LM340L Series 3-Terminal Positive Regulators

General Description

The LM140L series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. The LM140LA is an improved version of the LM78LXX series with a tighter output voltage tolerance (specified over the full military temperature range), higher ripple rejection, better regulation and lower quiescent current. The LM140LA regulators have ±2% V_{OUT} specification, 0.04%/V line regulation, and 0.01%/mA load regulation. When used as a zener diode/resistor combination replacement, the LM140LA usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM140LA to be used in logic systems, instrumentation, Hi-Fi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

The LM140LA/LM340LA are available in the low profile metal three lead TO-39 (H) and the LM340LA are also available in the plastic TO-92 (Z). With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shut-down circuit takes over, preventing the IC from overheating.

For applications requiring other voltages, see LM117L Data Sheet.

Features

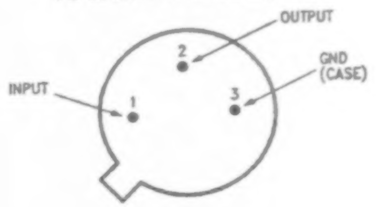
- Line regulation of 0.04%/V
- Load regulation of 0.01%/mA
- Output voltage tolerances of ±2% at T_j = 25°C and
  ±4% over the temperature range (LM140LA)
  ±3% over the temperature range (LM340LA)
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in metal TO-39 low profile package (LM140LA/LM340LA) and plastic TO-92 (LM340LA)

Output Voltage Options

LM140LA-5.0	5V	LM340LA-5.0	5V
LM140LA-12	12V	LM340LA-12	12V
LM140LA-15	15V	LM340LA-15	15V

Connection Diagrams

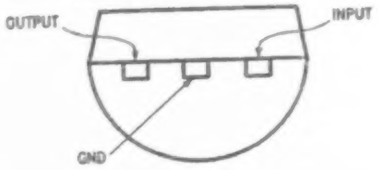
TO-39 Metal Can Package (H)



Bottom View

Order Number LM140LAH-5.0, LM140LAH-12, LM140LAH-15, LM340LAH-5.0, LM340LAH-12 or LM340LAH-15
See NS Package Number H03A

TO-92 Plastic Package (Z)



Bottom View

Order Number LM340LAZ-5.0, LM340LAZ-12 or LM340LAZ-15
See NS Package Number Z03A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 5)

Input Voltage	
5.0V, 12V, 15V Output Voltage Options	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	
LM140LA	−55°C to +125°C
LM340LA	0°C to +70°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	
Metal Can (H package)	−65°C to +150°C
Molded TO-92	−55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C
Plastic TO-92	+230°C

Electrical Characteristics (Note 2)

Test conditions unless otherwise specified. T_A = −55°C to +125°C (LM140LA), T_A = 0°C to +70°C (LM340LA), I_O = 40 mA, C_{IN} = 0.33 µF, C_O = 0.01 µF.

Output Voltage Option			5.0V			12V			15V			Units
Input Voltage (unless otherwise noted)			10V			19V			23V			
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	T_j = 25°C	4.9	5	5.1	11.75	12	12.25	14.7	15	15.3	V
	Output Voltage Over Temp. (Note 4)	LM140LA I_O = 1 − 100 mA	4.8		5.2	11.5		12.5	14.4		15.6	
			(7.2–20)			(14.5–27)			(17.6–30)			
		LM340LA I_O = 1 − 100 mA or I_O = 1 − 40 mA and V_{IN} = ( )V	4.85		5.15	11.65		12.35	14.55		15.45	
			(7–20)			(14.3–27)			(17.5–30)			
ΔV_O	Line Regulation	T_j = 25°C, I_O = 40 mA V_{IN} = ( )V		18	30		30	65		37	70	mV
			(7–25)			(14.2–30)			(17.3–30)			
		I_O = 100 mA V_{IN} = ( )V		18	30		30	65		37	70	
			(7.5–25)			(14.5–30)			(17.5–30)			
	Load Regulation	T_j = 25°C, I_O = 1 − 40 mA		5	20		10	40		12	50	
		I_O = 1 − 100 mA		20	40		30	80		35	100	
	Long Term Stability			12			24			30		mV 1000 hrs
I_O	Quiescent Current	T_j = 25°C		3	4.5		3	4.5		3.1	4.5	mA
		T_j = 125°C			4.2			4.2			4.2	
ΔI_Q	Quiescent Current Change	T_j = 25°C, ΔLoad I_O = 1 − 40 mA			0.1			0.1			0.1	mA
		ΔLine V_{IN} = ( )V			0.5			0.5			0.5	
			(7.5–25)			(14.3–30)			(17.5–30)			
V_N	Output Noise Voltage	T_j = 25°C (Note 3) f = 10 Hz–10 kHz		40			80			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz, V_{IN} = ( )V	55	62		47	54		45	52		dB
			(7.5–18)			(14.5–25)			(17.5–28.5)			
	Input Voltage Required to Maintain Line Regulation	T_j = 25°C, I_O = 40 mA	7			14.2			17.3			V

Note 1: Thermal resistance of H-package is typically 26°C/W θ_{JC}, 250°C/W θ_{JA} still air, and 94°C/W θ_{JA} 400 lf/min of air. For the Z-package is 60°C/W θ_{JC}, 232°C/W θ_{JA} still air, and 88°C/W θ_{JA} at 400 lf/min of air. The maximum junction temperature shall not exceed 125°C on electrical parameters.

Note 2: The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.

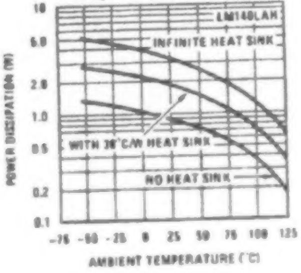
Note 3: It is recommended that a minimum load capacitor of 0.01 µF be used to limit the high frequency noise bandwidth.

Note 4: The temperature coefficient of V_{OUT} is typically within 0.01% V_O/°C.

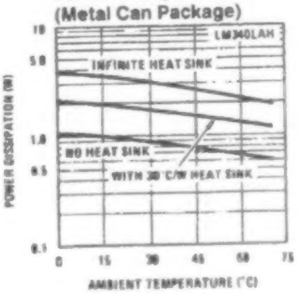
Note 5: Refer to RETS140-12H for LM140LAH-12, RETS140-15H for LM140LAH-15 or RETS140-15H for LM140LAH-5.0 military specification.

Typical Performance Characteristics

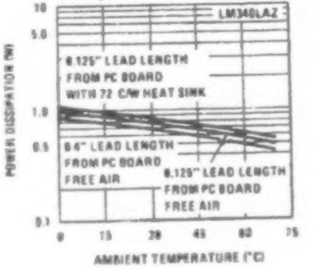
Maximum Average Power Dissipation



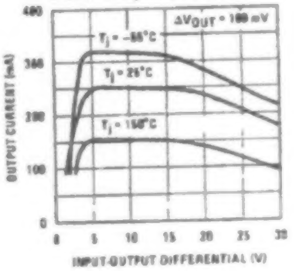
Maximum Average Power Dissipation (Metal Can Package)



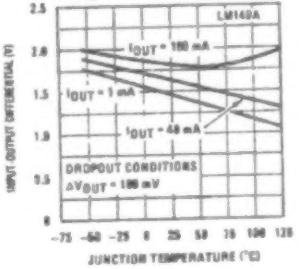
Maximum Average Power Dissipation (Plastic Package)



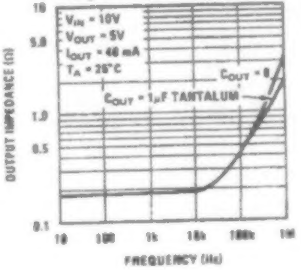
Peak Output Current



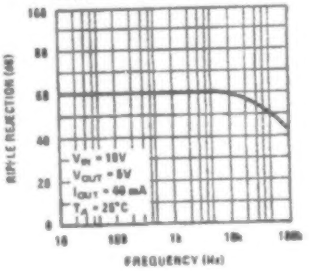
Dropout Voltage



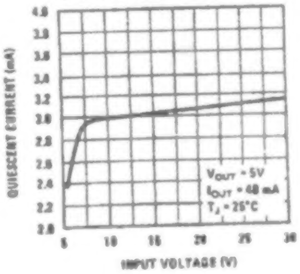
Output Impedance



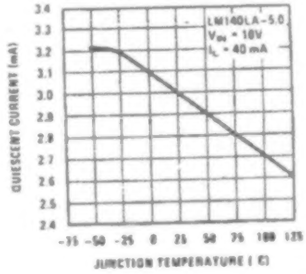
Ripple Rejection



Quiescent Current



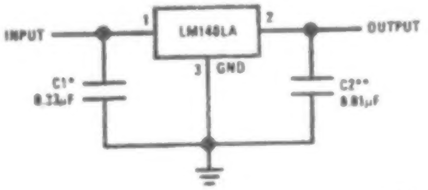
Quiescent Current



TL/H/7782-4

Typical Applications

Fixed Output Regulator

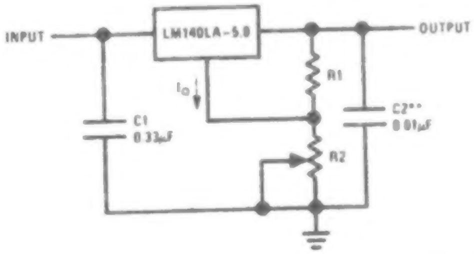

INPUT
1
LM140LA
2
OUTPUT
3
GND
C1*
0.33μF
C2**
0.01μF

TL/H/7782-5

*Required if the regulator is located far from the power supply filter

**See note 3 in the electrical characteristics table

Adjustable Output Regulator


INPUT
LM140LA-5.0
OUTPUT
IO
R1
R2
C1
0.33μF
C2**
0.01μF

TL/H/7782-6

$V_{OUT} = 5V + (5V/R1 + I_Q)\,R2$

$5V/R1 = 3\,I_Q$ load regulation (L_r) $[(R1 + R2)/R1]$ (L_r of LM140LA-5.0)

National
Semiconductor
Corporation

LM199/LM299/LM399/LM3999 Precision Reference

General Description

The LM199 series are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299 is rated for operation from −25°C to +85°C and the LM399 is rated from 0°C to +70°C.

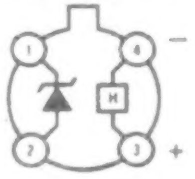
The LM3999 is packaged in a standard TO-92 package and is rated from 0°C to +70°C

Features

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400 μA
- Wide operating current — 500 μA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300 mW at 25°C
- Long term stability — 20 ppm
- Proven reliability, low-stress packaging in TO-46 integrated-circuit hermetic package, for low hysteresis after thermal cycling. 33 million hours MTBF at $T_A = +25°C$ ($T_J = +86°C$)
- Certified long term stability available

Connection Diagrams

Metal Can Package

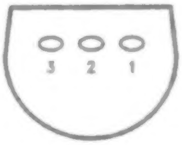


TL/H/5717-14

Top View

LM199/LM299/LM399 (See Table on fourth page)
NS Package Number H04D

Plastic Package TO-92



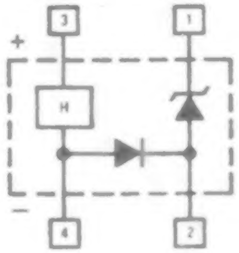
TL/H/5717-10

Bottom View

LM3999 (See Table on fourth page)
NS Package Number Z03A

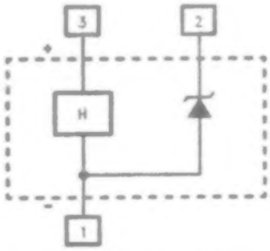
Functional Block Diagrams

LM199/LM299/LM399



TL/H/5717-15

LM3999



TL/H/5717-11

Absolute Maximum Ratings

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the following Reliability Electrical Test Specifications documents: RETS199X for LM199, RETS199AX for LM199A.

Temperature Stabilizer Voltage	
LM199/LM299/LM399	40V
LM3999	36V
Reverse Breakdown Current	20 mA
Forward Current	
LM199/LM299/LM399	1 mA
LM3999	−0.1 mA

Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	40V −0.1V
Operating Temperature Range	
LM199	−55°C to +125°C
LM299	−25°C to +85°C
LM399/LM3999	−0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
TO-92 package (10 sec.)	+260°C
TO-46 package (10 sec.)	+300°C

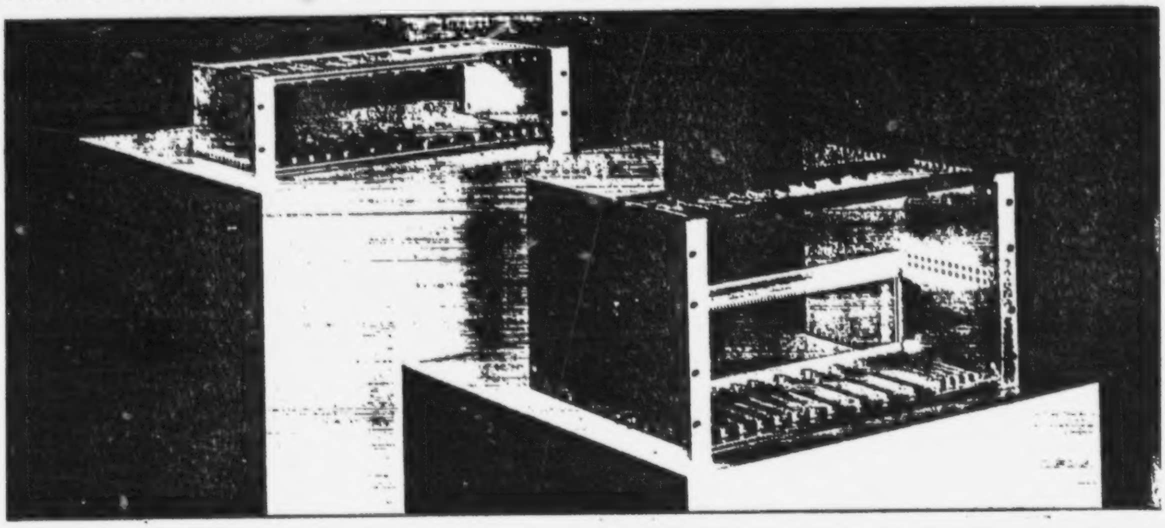
Electrical Characteristics (Note 2)

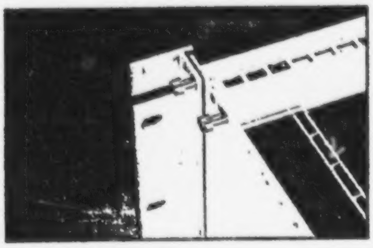
Parameter	Conditions	LM199/LM299			LM399			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$0.5\ mA \le I_R \le 10\ mA$	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change with Current	$0.5\ mA \le I_R \le 10\ mA$		6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le +85°C$ } LM199 $+85°C \le T_A \le +125°C$ } LM199 $-25°C \le T_A \le 85°C$ LM299 $0°C \le T_A \le +70°C$ LM399		0.00003 0.0005 0.00003 	0.0001 0.0015 0.0001 		 0.00003	 0.0002	%/°C %/°C %/°C %/°C
RMS Noise	$10\ Hz \le f \le 10\ kHz$		7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$ $T_A = -55°C$		8.5 22	14 28		8.5	15	mA
Temperature Stabilizer Supply Voltage		9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		3			3		sec.
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = +25°C$, (Note 3)		140	200		140	200	mA

Electrical Characteristics (Note 2)

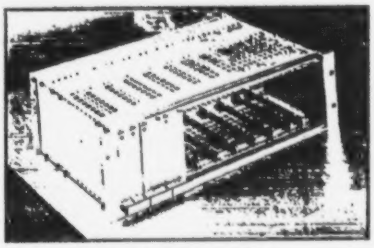
Parameter	Conditions	LM3999			Units
		Min	Typ	Max	
Reverse Breakdown Voltage	$0.6\ mA \le I_R \le 10\ mA$	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change with Current	$0.6\ mA \le I_R \le 10\ mA$		6	20	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.6	2.2	Ω
Reverse Breakdown Temperature Coefficient	$0°C \le T_A \le 70°C$		0.0002	0.0005	%/°C
RMS Noise	$10\ kHz \le f \le 10\ kHz$		7		μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		20		ppm
Temperature Stabilizer	$T_A = 25°C$, Still Air, $V_S = 30V$		12	18	mA
Temperature Stabilizer Supply Voltage				36	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		5		sec.
Initial Turn-On Current	$9 \le V_S \le 40$, $T_A = 25°C$		140	200	mA

KM6-II UNIVERSAL SUBRACKS

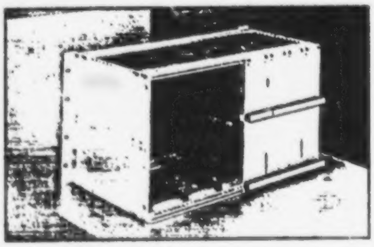




▲ TWO SCREW FIXING



▲ EMC CONVERSION (see page 3.09)



▲ REVERSED SUBRACK

FEATURES

- Strong and versatile
- Two screw fixing of tie bars
- Conforms to IEC 297-3
- Total versatility permits wide range of configurations
- Available in kit or piece-part form
- Accurate location for first time assembly
- Rugged construction
- Pre-tapped holes and machine screws throughout
- EMC conversion (see page 3.09)
- No location mouldings
- With or without front handles

KM6-II Universal Subracks are strong, versatile and easy to assemble.

The tie bars are of large section for rigidity and are secured using two fixing screws into counterbored holes. The screws thus act as location dowels giving a high degree of accuracy.

This version, as the name implies, has the capability of housing Eurocards of different sizes in a variety of configurations.

The frame can be constructed from standard parts in 3U, 4U, 5U, 6U and 9U heights.

The endplates, 240mm, 300mm, 360mm or 420mm deep, incorporate a series of punched holes so that the tie bars can be assembled at any required

84 HP variants are offered in Backplane or DIN 41612 connector mounting and are supplied with or without front handles. DIN 41612 rear tie bars are fully tapped.

Please note 4U and 5U versions can only be ordered from piece parts. Alternative versions of 3U, 6U and 9U subracks can also be ordered from piece parts.

Location mouldings are no longer required, thus improving assembly time.

ORDER SEPARATELY

DIN 41612 connector frame	3.18
EMC conversion	3.09
Guides	3.17
Divider kits	3.19
Dust covers	3.22
Horizontal mounting	3.23
Backplane spacers	3.16

NB. The conductive finish gives excellent electrical conductivity but is more easily marked than anodising. During assembly care should therefore be taken to avoid the deposition of grease and oil, particularly on visible surfaces.

MATERIAL SPECIFICATION

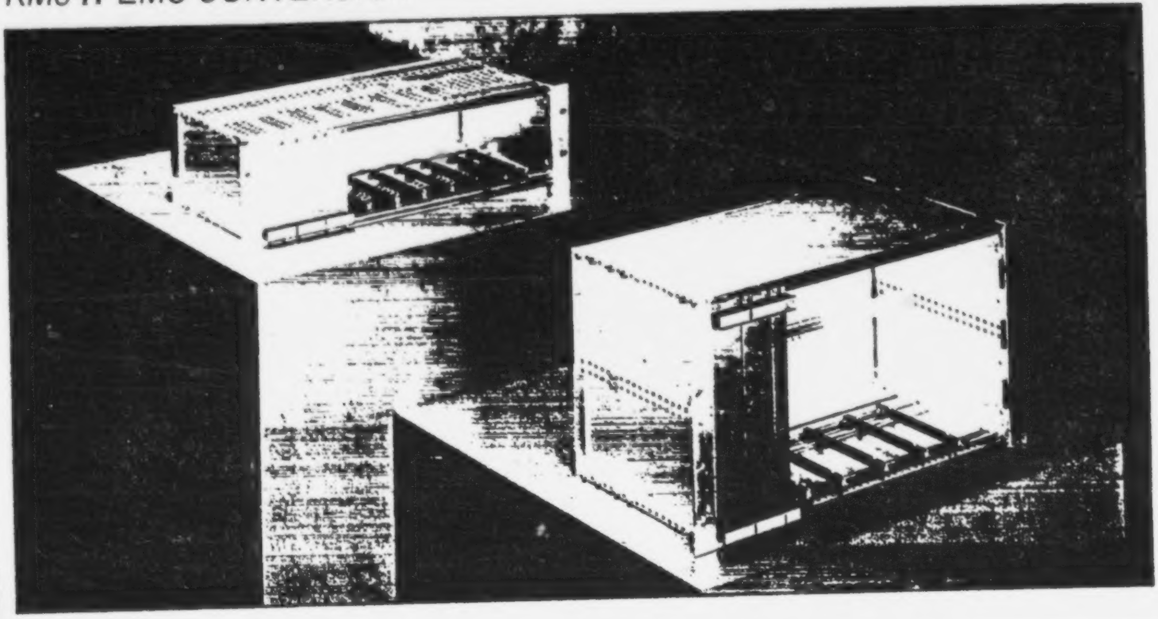
All extrusions	: Aluminium alloy BS 1474HE9TF
End plates	: 2 & 2,5mm aluminium BS 1470 NS4 1/2H
Tapped strips	: MS zinc pass.
Finish	: Conductive, except rack mounting angles and handles (anodised)

CONTENTS OF KIT

2 end plates
2 end plate angles
2 front extrusions
All fixings
Assembly instructions

Rear tie bars -	2 - 3U 3 - 6U 4 - 9U
Tapped strips:	
Backplane variants-	4 - 3U 6 - 6U 8 - 9U
DIN 41612 variants-	2

KM6-II EMC CONVERSION



EMC CONVERSION KITS FOR KM6-II UNIVERSAL SUBRACKS

These EMC Conversion kits enable KM6-II Universal Subracks to be converted to EMC Subracks without modification and at little extra cost.

The kits comprise a range of components, including top and base covers, rear closing angles and full or individual panels.

The benefit of this system is that it allows the designer the flexibility of using the Universal Subracks as normal or converting them at little extra cost if an EMC problem is discovered or local legislation demands it.

WHAT MUST I ORDER TO ACHIEVE AN EMC SUBRACK?
1 KM6-II Universal Subrack;
1 EMC conversion kit;
Individual or full width panels, front and rear
(to suit requirements).

KM6-II UNIVERSAL SUBRACKS

For 160mm BOARDS

Ordering information

End plate	For ordering information see page 3.08
3U x 240mm	
6U x 240mm	
9U x 240mm	

FOR 160 OR 220MM BOARDS

3U x 300mm	For ordering information see page 3.08
6U x 300mm	
3U x 360mm	
6U x 360mm	
9U x 360mm	

FOR 280 or 340MM BOARDS

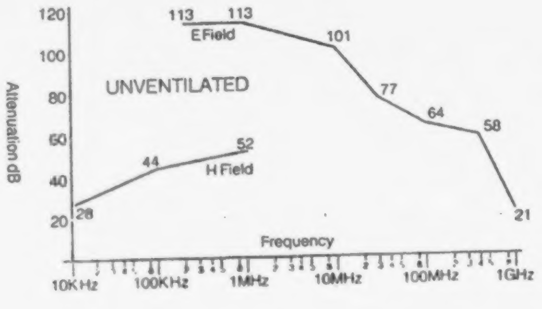
6U x 420mm	For ordering information

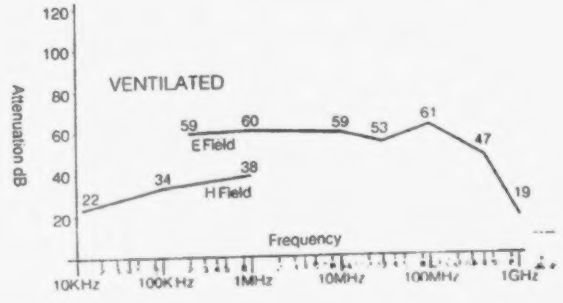
TYPICAL SHIELDING PERFORMANCE

These performance figures were obtained by testing a representative sample from production batches. The tests carried out were in accordance with MIL - STD - 285 modified where necessary due to the nature of the subracks. The figures are given as a guideline. Any additions or modifications will have an effect upon the shielding performance and it is essential, therefore, that these units are retested once all the equipment has been mounted into them.

Performance figures were obtained from subracks fitted with full width EMC panels front and rear, reading from the top panel.

Figures stated were obtained from our in-house test facility.
E : FIELD : Denotes electric field
H : FIELD : Denotes magnetic field





EMC

This kit
84HP s
panels.

CONTE

2 plain
2 tappe
2 rear c
Top ar
unventil
End pla
or 20 or
EMC C
end pla

Height
3U
3U
6U
6U
9U
9U

EMC C
300mm

Height
3U
3U
6U
6U

EMC CC
360mm

Height
3U
3U
6U
6U
9U
9U

EMC CO
420mm

Height
6U
6U
9U
9U

ADDIT

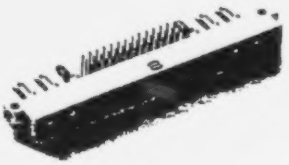
Two type
supplied i
as repla
performa

Type 1 is
be fitted b
front divid

Gds A-M DIN 41 612 · VG 95 324 · Type M

Number of contacts

78+2, 60+4, 42+6, 24+8

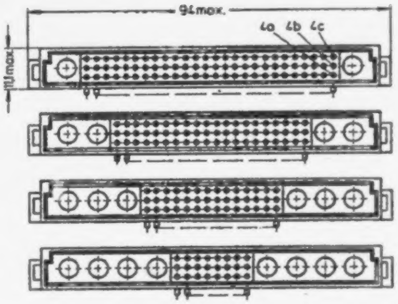


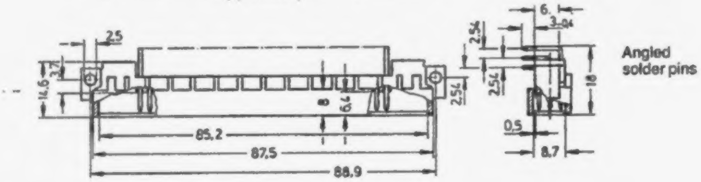
Male connectors

Part No. Performance levels according to DIN 41 612, explanations page 10

Identification	Number of contacts	Contact arrangement	3	2	1
Male connector with angled solder pins			09 03 178 7901	09 03 178 6901	09 03 178 2901*
			09 03 160 7901	09 03 160 6901	09 03 160 2901*
			09 03 142 7901	09 03 142 6901	09 03 142 2901*
			09 03 124 7901	09 03 124 6901	09 03 124 2901*

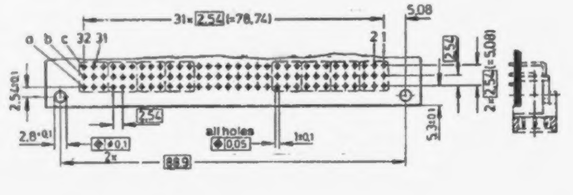
Dimensions


94max.
4a 4b 4c
11,5max


2,5
3,7
14,6
8
6,4
85,2
87,5
88,9
2,54
2,54
2,54
6
3-0,4
18
0,5
8,7
Angled solder pins

Order separately high current, high voltage, coaxial and fibre optic contacts, see page 42

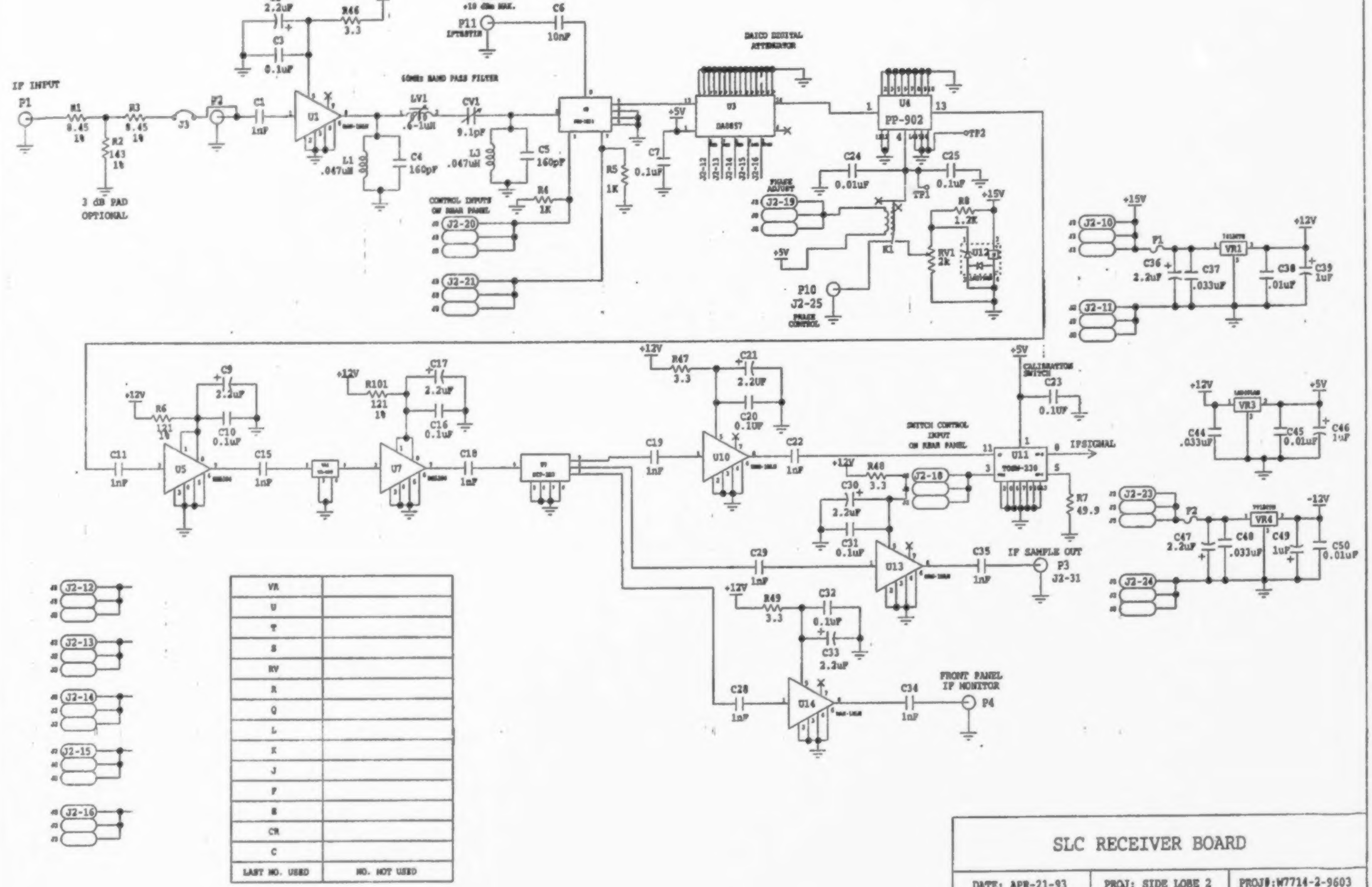
Board drillings


31×2,54(=78,74)
5,08
a b c 32 31
2 1
2,54±0,1
2,54
2,8+0,1
⌖ Ø0,1
2×
all holes
⌖ 0,05
1±0,1
88,9
5,3±0,1
2,54
2×2,54(=5,08)

Dimensions in mm

APPENDIX B

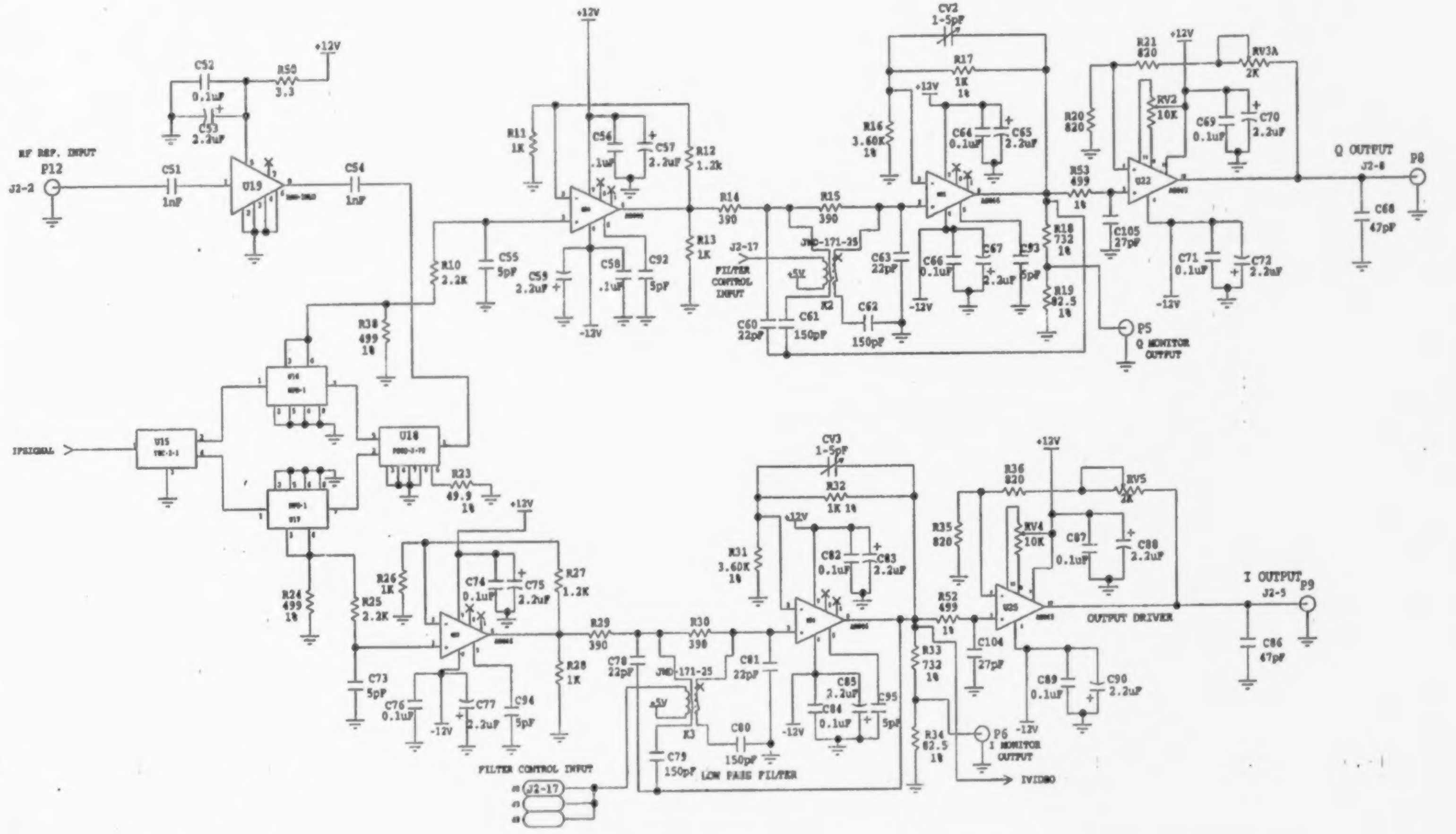
IF RECEIVER SCHEMATICS


IF INPUT
P1
R1 8.45 1%
R2 143 1%
R3 8.45 1%
3 dB PAD OPTIONAL
J3
P2
C1 1nF
C2 2.2uF
C3 0.1uF
R46 3.3
+12V
U1
60MHz BAND PASS FILTER
LV1 .6-1uH
L1 .047uH
C4 160pF
CV1 9.1pF
L3 .047uH
C5 160pF
R4 1K
IF TEST IN +10 dBm MAX.
P11 IFTESTIN
C6 10nF
R5 1K
C7 0.1uF
+5V
CONTROL INPUTS ON REAR PANEL
J2-20
J2-21
DAICO DIGITAL ATTENUATOR
U3 DA0857
J2-12
J2-13
J2-14
J2-15
J2-16
U4 PP-902
1
13
4
TP2
TP1
C24 0.01uF
C25 0.1uF
PHASE ADJUST
J2-19
K1
R8 1.2K
+15V
RV1 2k
U12
P10 J2-25 PHASE CONTROL
J2-10
J2-11
F1
C36 2.2uF
C37 .033uF
VR1
C38 .01uF
C39 1uF
U5
R6 121 1%
C9 2.2uF
C10 0.1uF
C11 1nF
C15 1nF
U7
R101 121 1%
C17 2.2uF
C16 0.1uF
C18 1nF
C19 1nF
U10
R47 3.3
C21 2.2UF
C20 0.10UF
C22 1nF
SWITCH CONTROL INPUT ON REAR PANEL
CALIBRATION SWITCH
C23 0.10UF
U11 TOSW-230
11
8
3
5
IFSIGNAL
R7 49.9
R48 3.3
J2-18
C30 2.2uF
C31 0.1uF
C29 1nF
U13
C35 1nF
IF SAMPLE OUT
P3 J2-31
R49 3.3
C32 0.1uF
C33 2.2uF
C28 1nF
U14
C34 1nF
FRONT PANEL IF MONITOR
P4
VR3
C44 .033uF
C45 0.01uF
C46 1uF
J2-23
J2-24
F2
C47 2.2uF
C48 .033uF
VR4
C49 1uF
C50 0.01uF
-12V

LAST NO. USED	NO. NOT USED
VR	
U	
T	
S	
RV	
R	
Q	
L	
K	
J	
F	
E	
CR	
C	

SLC RECEIVER BOARD

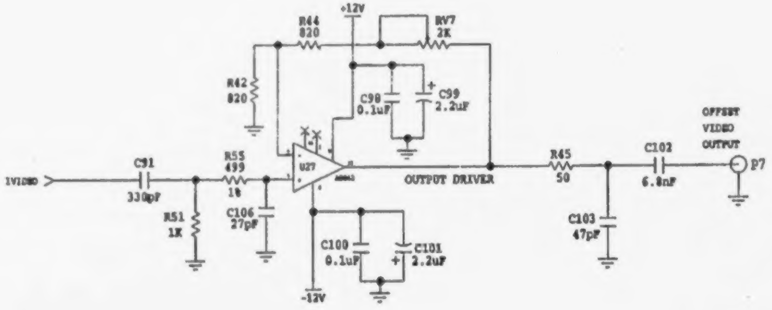
DATE: APR-21-93	PROJ: SIDE LOBE 2	PROJ#:W7714-2-9603
	DRAWN BY: PW DATE: APR-21-93	SHEET 1 OF 3


RF REF. INPUT
J2-2
P12
C51 1nF
C52 0.1uF
C53 2.2uF
R50 3.3
+12V
U19
C54 1nF
R10 2.2K
C55 5pF
R38 499 1%
R11 1K
C56 .1uF
C57 2.2uF
C59 2.2uF
C58 .1uF
C92 5pF
-12V
R12 1.2k
R13 1K
R14 390
R15 390
J2-17
FILTER CONTROL INPUT
+5V
JMD-171-25
K2
C60 22pF
C61 150pF
C62 150pF
C63 22pF
CV2 1-5pF
R17 1K 1%
R16 3.60K 1%
C64 0.1uF
C65 2.2uF
C66 0.1uF
C67 2.2uF
C93 5pF
R18 732 1%
R19 82.5 1%
R53 499 1%
C105 27pF
P5
Q MONITOR OUTPUT
R20 820
R21 820
RV2 10K
RV3A 2K
C69 0.1uF
C70 2.2uF
U22
C71 0.1uF
C72 2.2uF
Q OUTPUT
J2-8
P8
C68 47pF
IPSIGNAL
U15
U16
U17
U18
R23 49.9 1%
R24 499 1%
R25 2.2K
R26 1K
C73 5pF
C74 0.1uF
C75 2.2uF
C76 0.1uF
C77 2.2uF
C94 5pF
R27 1.2K
R28 1K
R29 390
R30 390
C78 22pF
JMD-171-25
K3
C79 150pF
C80 150pF
C81 22pF
LOW PASS FILTER
FILTER CONTROL INPUT
J2-17
CV3 1-5pF
R32 1K 1%
R31 3.60K 1%
C82 0.1uF
C83 2.2uF
C84 0.1uF
C85 2.2uF
C95 5pF
R33 732 1%
R34 82.5 1%
P6
I MONITOR OUTPUT
IVIDEO
R52 499 1%
C104 27pF
R35 820
R36 820
RV4 10K
RV5 2K
C87 0.1uF
C88 2.2uF
U25
OUTPUT DRIVER
C89 0.1uF
C90 2.2uF
I OUTPUT
J2-5
P9
C86 47pF

SLC RECEIVER BOARD

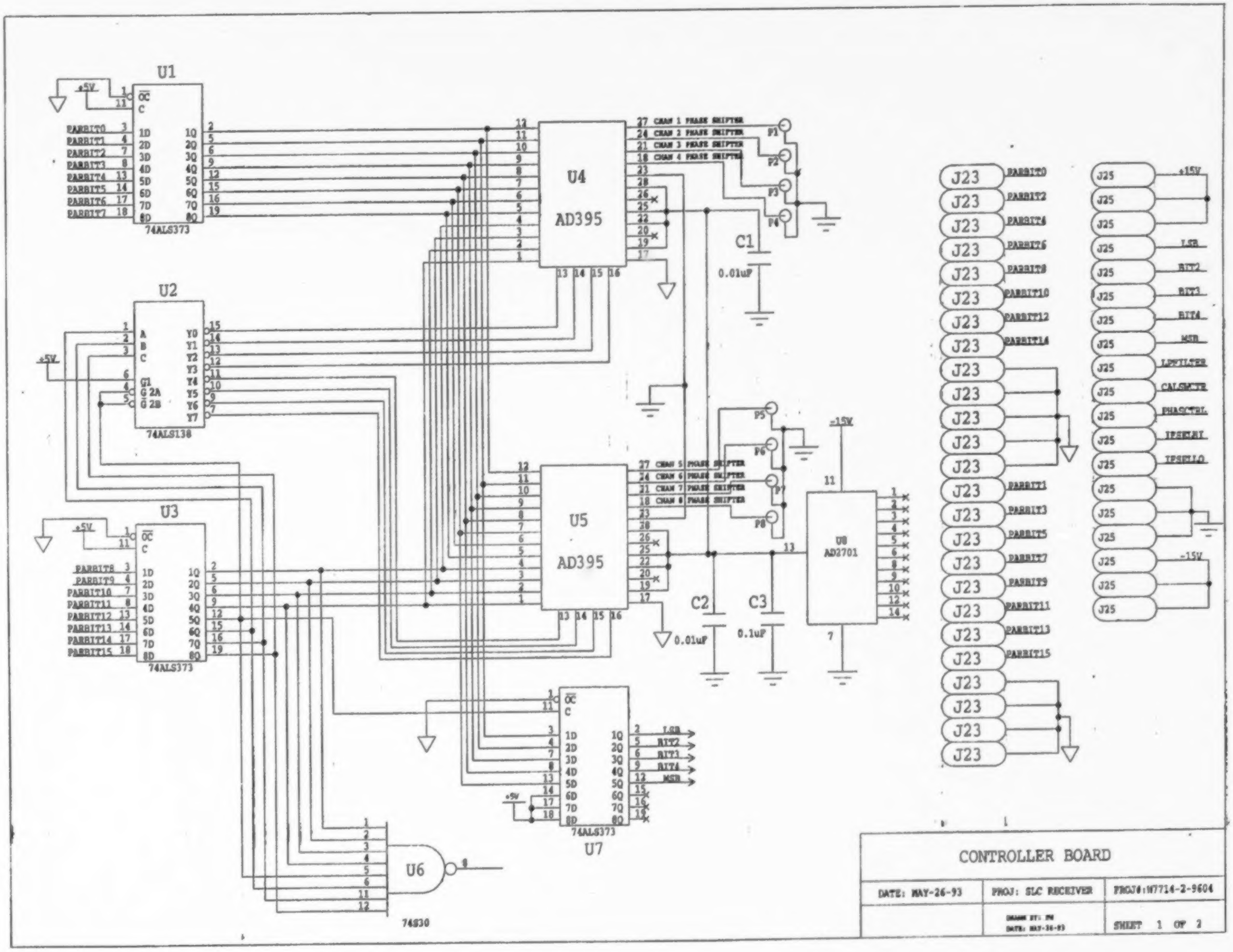
DATE: APR-21-93
PROJ: SIDE LOBE 2
PROJ#: 7714-2-9603

DRAWN BY: PH
DATE: APR-21-93
SHEET 2 OF 3


+12V
R44
820
RV7
2K
R42
820
C98
0.1uF
C99
2.2uF
OFFSET
VIDEO
OUTPUT
C102
6.8nF
P7
1VIDEO
C91
330pF
R55
499
1%
U27
OUTPUT DRIVER
R45
50
R51
1K
C106
27pF
C103
47pF
C100
0.1uF
C101
2.2uF
-12V

SLC RECEIVER BOARD

DATE: APR-21-93	PROJ: SIDE LOBE 2	PROJ#: 7714-2-9603
	DRAWN BY: [illegible] DATE: APR-21-93	SHEET 3 OF 3

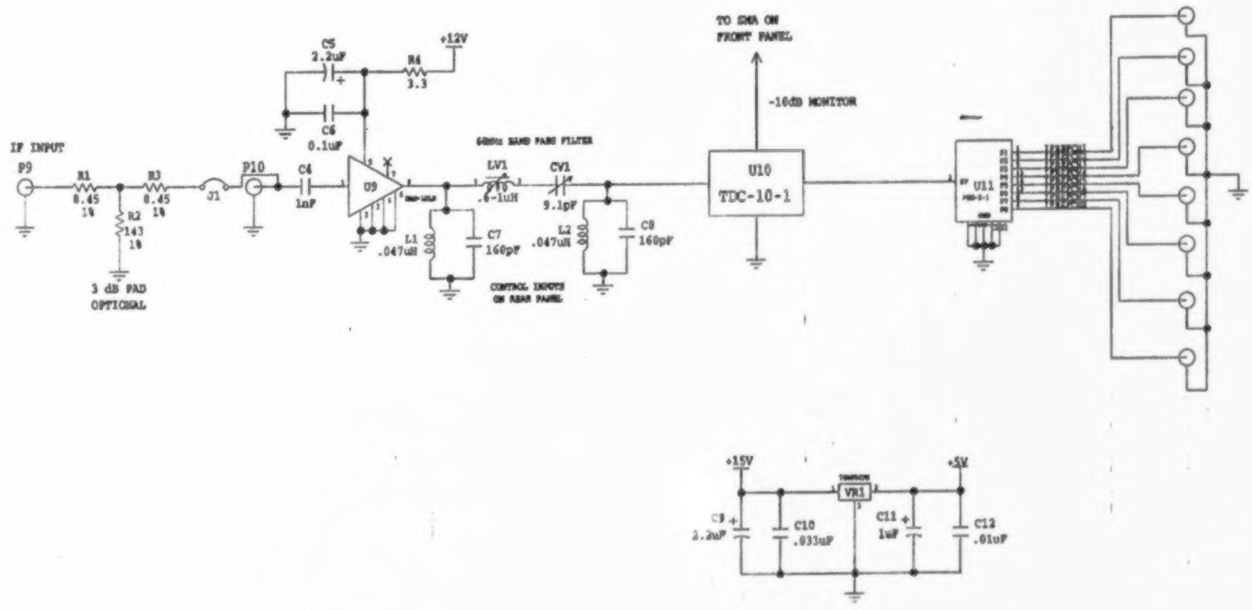

U1
74ALS373
PARBIT0
PARBIT1
PARBIT2
PARBIT3
PARBIT4
PARBIT5
PARBIT6
PARBIT7
+5V
U2
74ALS138
U3
74ALS373
PARBIT8
PARBIT9
PARBIT10
PARBIT11
PARBIT12
PARBIT13
PARBIT14
PARBIT15
U4
AD395
CHAN 1 PHASE SHIFTER
CHAN 2 PHASE SHIFTER
CHAN 3 PHASE SHIFTER
CHAN 4 PHASE SHIFTER
P1
P2
P3
P4
C1
0.01uF
U5
AD395
CHAN 5 PHASE SHIFTER
CHAN 6 PHASE SHIFTER
CHAN 7 PHASE SHIFTER
CHAN 8 PHASE SHIFTER
P5
P6
P7
P8
C2
0.01uF
C3
0.1uF
U8
AD2701
-15V
U7
74ALS373
LSB
BIT2
BIT3
BIT4
MSB
U6
74S30
J23
J25
+15V
LPFILTER
CALSWCTR
PHASCTRL
IFSELHI
IFSELLO

CONTROLLER BOARD

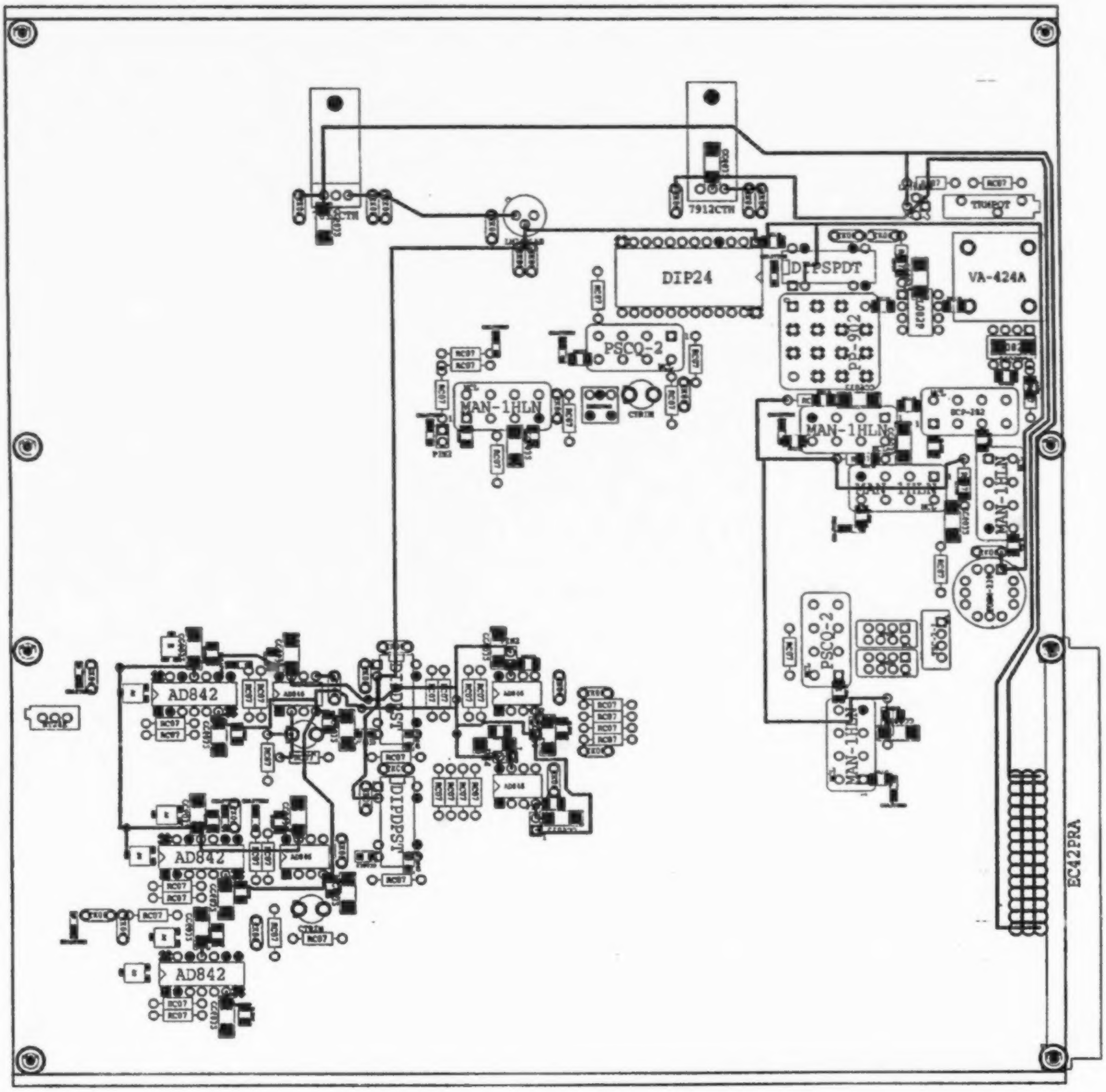
DATE: MAY-26-93 | PROJ: SLC RECEIVER | PROJ#:N7714-2-9604

DRAWN BY: PW
DATE: MAY-26-93

SHEET 1 OF 2


IF INPUT
P9
R1
8.45
1%
R2
143
1%
3 dB PAD
OPTIONAL
R3
8.45
1%
J1
P10
C4
1nF
C5
2.2uF
C6
0.1uF
R4
3.3
+12V
U9
60MHz BAND PASS FILTER
LV1
.6-1uH
CV1
9.1pF
L1
.047uH
C7
160pF
L2
.047uH
C8
160pF
CONTROL INPUTS
ON REAR PANEL
TO SMA ON
FRONT PANEL
-10dB MONITOR
U10
TDC-10-1
U11
+15V
C9
2.2uF
C10
.033uF
VR1
C11
1uF
C12
.01uF
+5V

CONTROLLER BOARD		
DATE: MAY-26-93	PROJ: SLC RECEIVER	PROJ#:W7714-2-9604
	DRAWN BY: PW DATE: MAY-26-93	SHEET 2 OF 2


DIP24
DIPSPDT
VA-424A
7912CTH
TRMPOT
PSCO-2
MAN-1HLN
MAN-1HLN
MAN-1HLN
MAN-1HLN
MAN-1HLN
PSCO-2
AD842
AD842
AD842
DIPDPST
DIPDPST
EC42PRA
RC07

RECEIVER BOARD LAYOUT (NOT TO SCALE)

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FINAL DESIGN REPORT (ver 1.2)

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This report is the final design report for the Side-Lobe Canceller (SLC) 60 megahertz IF receiver system. It presents the detailed designs and calculations for each section of the IF receiver. Numerous diagrams are used and the three page schematic diagram is included as an appendix. This report presents the design before final prototype testing, therefore the design is subject to minor changes following testing.

The Side-Lobe Canceller IF receiver consists of a series of eight identical boards, one for each channel of the SLC array. Each board is capable of producing one I and one Q output at a level that is suitable for digitizing by a data acquisition system. In addition, the boards provide monitor points and a high level 60 MHz output, suitable for future digital sampling. Each board also has an offset video output, with a bandwidth of one to six megahertz. The receiver enclosure is mounted in a rack in the portable laboratory, close to the data acquisition systems its outputs are connected to. The eight channel receiver boards are mounted in a double height eurocard rack, with a ninth board for the computer interface, reference amplifier and splitter. All IF and video connections are made at the rear of the enclosure, with a backplane assembly for power and control signals.

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Side-Lobe Canceller (SLC)
IF Receiver
Beam Forming Network (BFN)
Noise Figure
Offset Video
Bandpass Filter
Digital Attenuator
Quadrature Phase Detector
Bessel Low Pass Filter
Sallen-Key Filter Circuit
Voltage Variable Phase Shifter (VVPS)
Analogue-to-Digital Converter (ADC)

#508983